


LCFC Confidential

Y550 M/B Schematics Document

Comet Lake H-Processor with DDR4 + NV N18E-G1/G0 GPU

2019-07-24

REV: 0.1

Security Classification		LC Future Center Secret Data		Title		
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Cover Page		
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
7000P@	7000P stuff
7502M@	7502 stuff
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
AG@	Anti-ghost
AOAC@	AOAC support part
BL@	BL
CD@	Cost down part
CNVI@	CNVI support part
DCI@	DCI
Debug@	USB2.0 port 1for Debug
EMC@	EMC part
EMC_8111H@	LAN 8111H EMC Part
EMC_NS@	EMC not stuff
GC6@	GC6
GYSNC@	GYSNC support part
HDMI@	HDMI
i5@i7@i9@	CPU Part
ME@	ME part(connector, hole)
M6GX6@S6GX6@	VRAM part

BOM Structure	BTO Item
MIRROR@	MIRROR
N18EG0@N18EG1@	GPU part
NOMIRROR@	17'' stuff
NPI@	SPI VCC diode stuff
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
UP9632_@	UP9632 part stuff
USB@	USB2.0 port1 for USB Port
X76@	VRAM
GS@	Reserved for G-sensor

Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7	RGBKB
9	AG
10	Back USB3.0
11:13	NA
14	BT

Port	Function
1	Back USB3.0
2	Right USB3.0
3	Left USB3.0
4	Type-C Port
5	Back USB3.0
6	NA

Port	Function
0A	NA
0B	HDD Gen3
1A	M.2 SSD Gen3
1B	NA
2	NA
3	NA
4	M.2 SSD Gen3
5	NA
7	NA

Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
14	WLAN Gen1
15	LAN Gen1
16	for Card Reader 17"
17:20	M.2 SSD

24 PCIE_CRX_GTX_N[0..15]

24 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15] 24

PCIE_CTX_C_GRX_P[0..15] 24

VCCIO

Note:
Place R_comp inside CPU cavity
Trace width>=12 mils ,Min Spacing>15mil
Max length<400 mils.

19 DMI_CRX_PTX_P0 DMI_CRX_PTX_P0 D8
19 DMI_CRX_PTX_N0 DMI_CRX_PTX_N0 E8
19 DMI_CRX_PTX_P1 DMI_CRX_PTX_P1 E6
19 DMI_CRX_PTX_N1 DMI_CRX_PTX_N1 F6
19 DMI_CRX_PTX_P2 DMI_CRX_PTX_P2 D5
19 DMI_CRX_PTX_N2 DMI_CRX_PTX_N2 E5
19 DMI_CRX_PTX_P3 DMI_CRX_PTX_P3 J8
19 DMI_CRX_PTX_N3 DMI_CRX_PTX_N3 J8

UC1C

PEG_RXP_0 PEG_TXP_0
PEG_RXN_0 PEG_TXN_0
PEG_RXP_1 PEG_TXP_1
PEG_RXN_1 PEG_TXN_1
PEG_RXP_2 PEG_TXP_2
PEG_RXN_2 PEG_TXN_2
PEG_RXP_3 PEG_TXP_3
PEG_RXN_3 PEG_TXN_3
PEG_RXP_4 PEG_TXP_4
PEG_RXN_4 PEG_TXN_4
PEG_RXP_5 PEG_TXP_5
PEG_RXN_5 PEG_TXN_5
PEG_RXP_6 PEG_TXP_6
PEG_RXN_6 PEG_TXN_6
PEG_RXP_7 PEG_TXP_7
PEG_RXN_7 PEG_TXN_7
PEG_RXP_8 PEG_TXP_8
PEG_RXN_8 PEG_TXN_8
PEG_RXP_9 PEG_TXP_9
PEG_RXN_9 PEG_TXN_9
PEG_RXP_10 PEG_TXP_10
PEG_RXN_10 PEG_TXN_10
PEG_RXP_11 PEG_TXP_11
PEG_RXN_11 PEG_TXN_11
PEG_RXP_12 PEG_TXP_12
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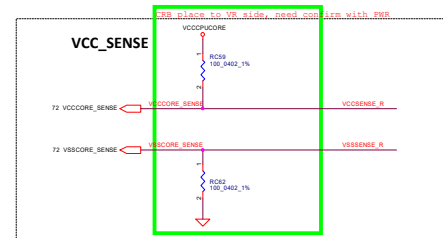
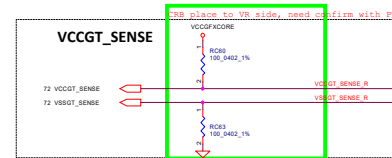
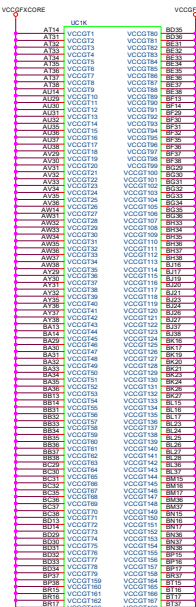
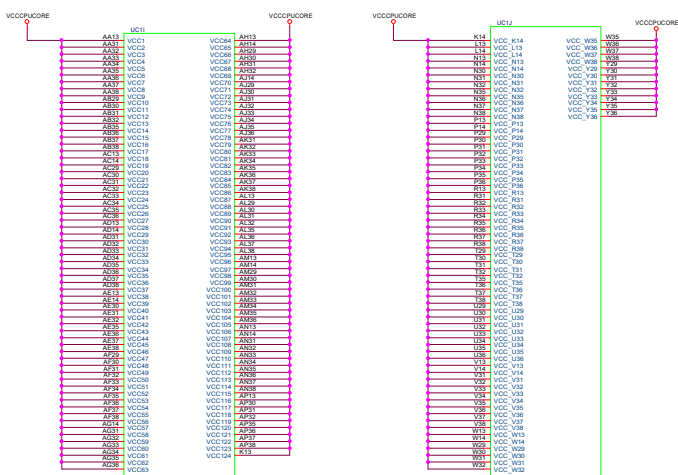
PEG_COMP G2

PEG_RCOMP

COMETLAKE-H-CPU_BGA1440

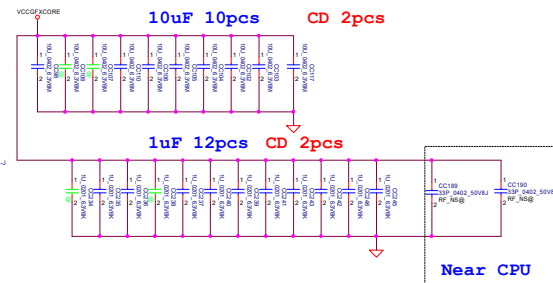
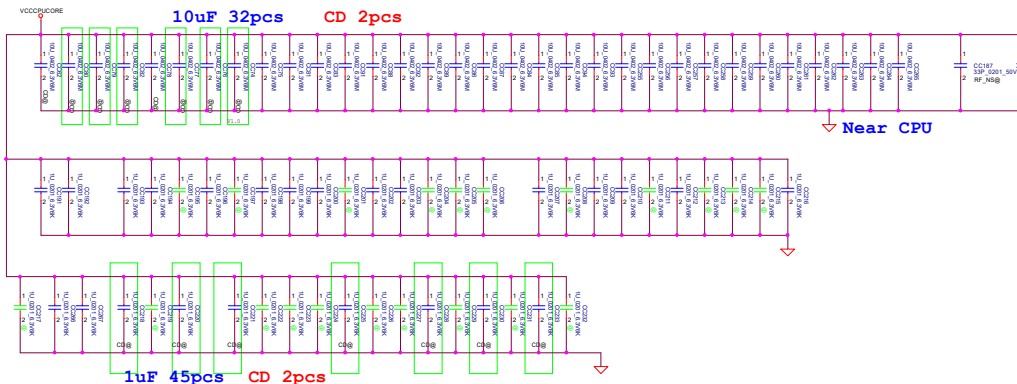
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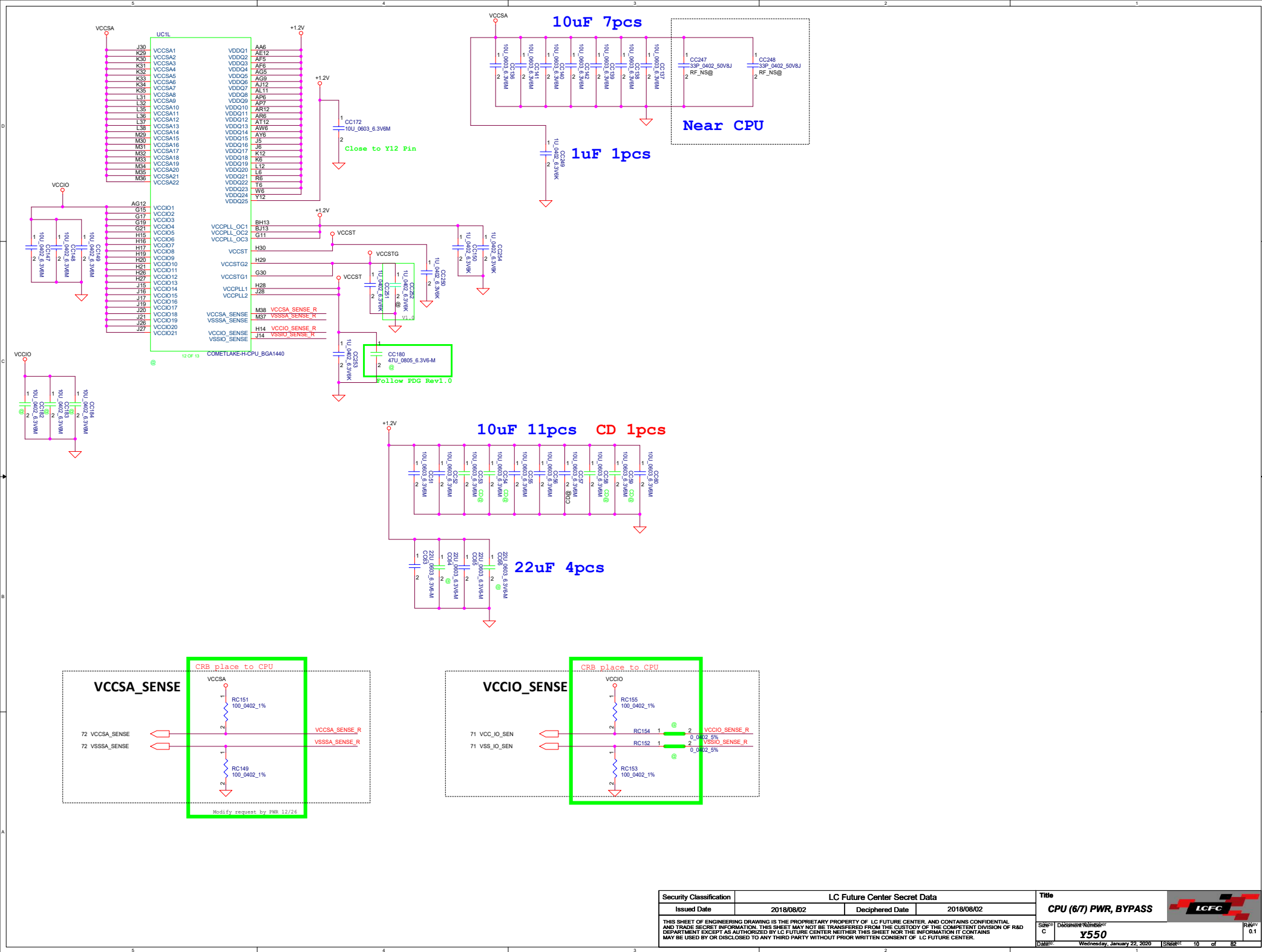
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A25 PCIE_CTX_GRX_N15 OPT@ CC16 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N15
B24 PCIE_CTX_GRX_P14 OPT@ CC31 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P14
C24 PCIE_CTX_GRX_N14 OPT@ CC15 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N14
B23 PCIE_CTX_GRX_P13 OPT@ CC30 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P13
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C18 PCIE_CTX_GRX_N8 OPT@ CC9 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N8
A17 PCIE_CTX_GRX_P7 OPT@ CC24 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P7
B17 PCIE_CTX_GRX_N7 OPT@ CC8 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N7
C16 PCIE_CTX_GRX_P6 OPT@ CC23 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P6
B16 PCIE_CTX_GRX_N6 OPT@ CC7 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N6
A15 PCIE_CTX_GRX_P5 OPT@ CC22 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P5
B15 PCIE_CTX_GRX_N5 OPT@ CC6 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N5
C14 PCIE_CTX_GRX_P4 OPT@ CC21 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_P4
B14 PCIE_CTX_GRX_N4 OPT@ CC5 1 2 0.22U 0201 6.3V6-K PCIE_CTX_C_GRX_N4
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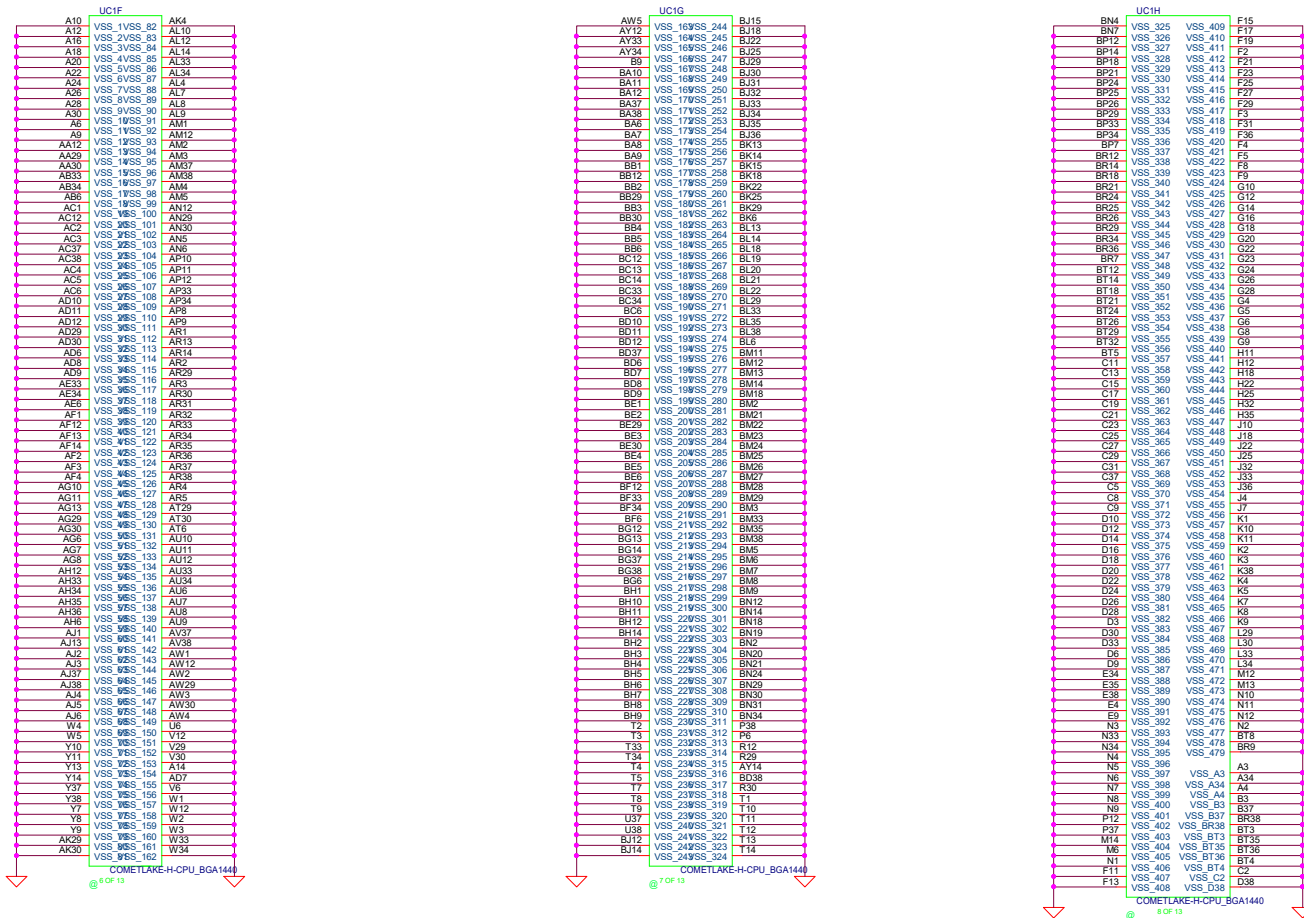


PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45

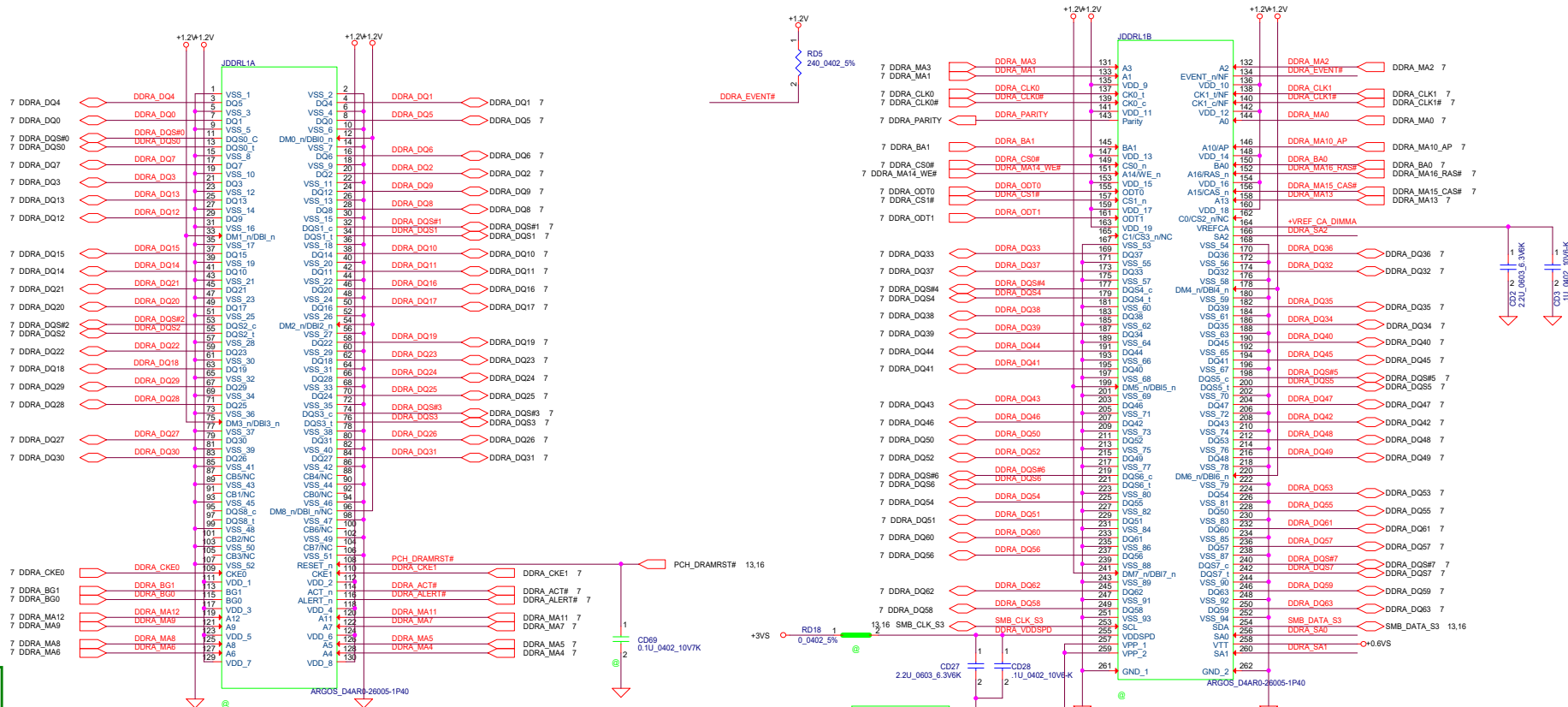
PDG near: 470uf*4 47uf*20
backside:10uf*32 1uf*45



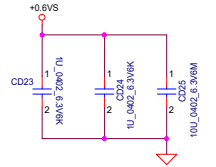




DDR4 SO-DIMM A



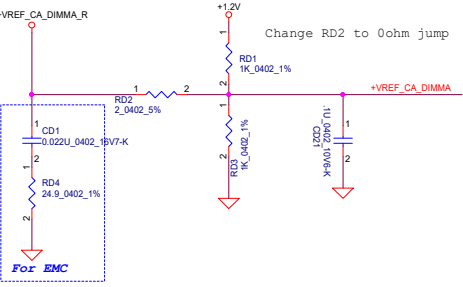
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Place near DIMM



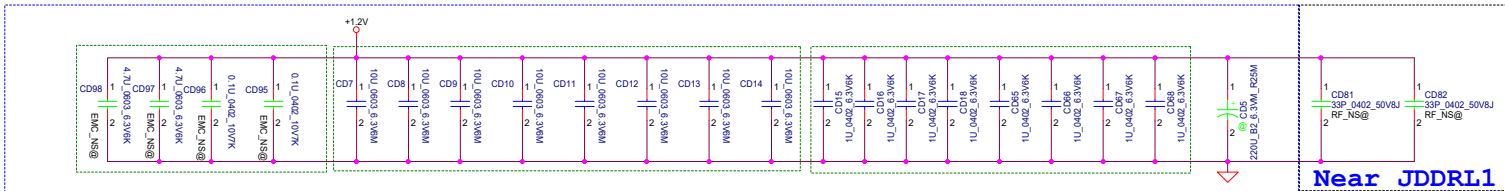
Note: VREF trace width: 20 mils at least
Spacing: 20 mils to other signal/planes
Place near DIMM socket

SPD Address = 0H

Layout Note:
Place near DIMM

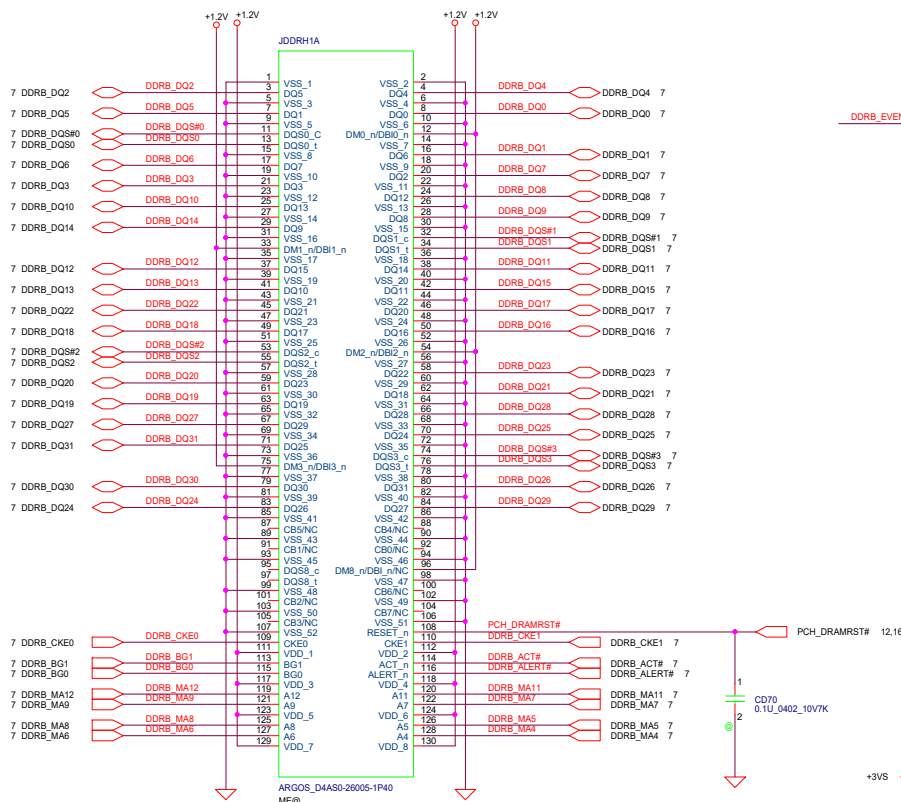


For EMC



Near JDDR18

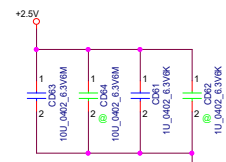
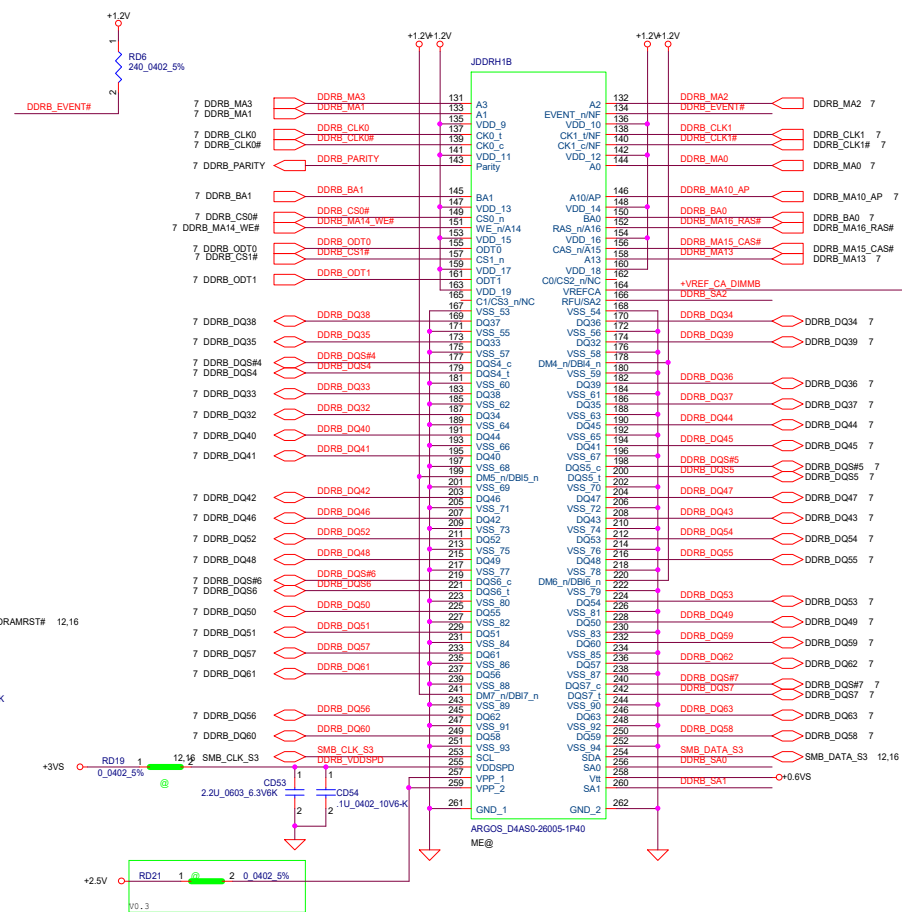
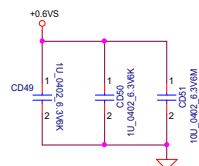
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DDR4 SO-DIMM B

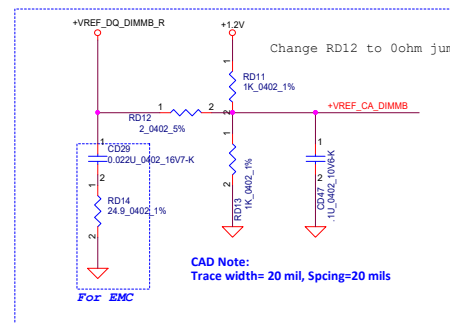
SPD Address = 2H




Layout Note:
Place near D

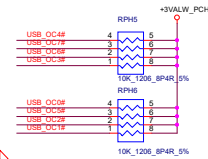
Layout Note:
Place near DIMM




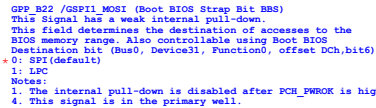
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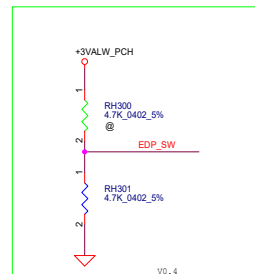
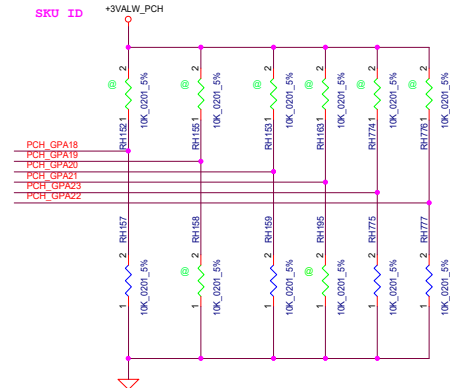
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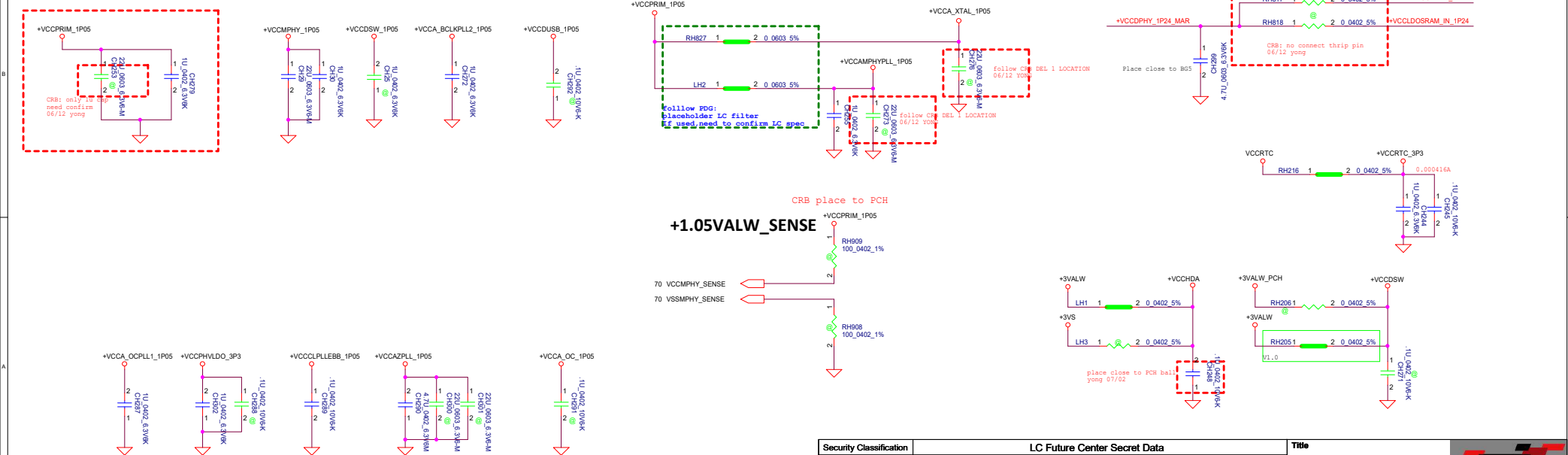
Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC

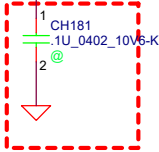



Board ID table need modify
yong 07/10

```
PCH_GPA22 add for distinguish
L350: H
Y550:L
yong 07/11
```

Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22 (L340: H Y550: I)	PCH_GPA23 (Reserved)
Y550-15-N18E G0	0	0	0	0	0	0
Y550-15-N18E G1-B	0	0	0	1	0	0
Y550-15-N18P G61	0	0	1	0	0	0
Y550-15-N18P G62	0	0	1	1	0	0
Y540-17-N18E G0	0	1	0	0	0	0
Y540-17-N18E G1-B	0	1	0	1	0	0
Y540-17-N18P G61	0	1	1	0	0	0
Y540-17-N18P G62	0	1	1	1	0	0



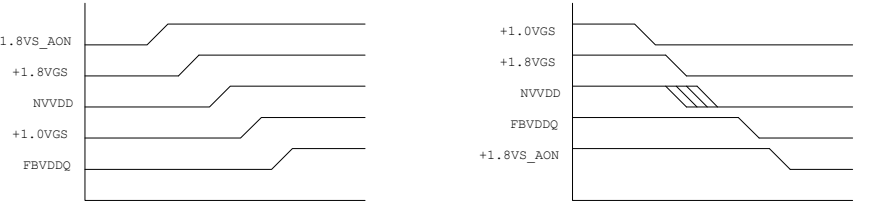


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N18E-G1 GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVDD_PWM_VID	PWM Output to control NVDD	NVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	GC6 FRAME BUFFER ENABLE	FB_GC6_EN	(10K pull down)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K pull High)
GPIO3	OUT	UNUSED	UNUSED	UNUSED	
GPIO4	OUT	GC6:1V8_MAIN_EN	GPU power sequencing for GC6 --- 1V8_MAIN_EN	1V8_MAIN_EN	(10K pull High)
GPIO5	IN	FRAME_LOCK*	Active low Frame Lock for NVSR panel	GPU_FRAME_LOCK#	
GPIO6	OUT	NVDD_PSI*	Phase Shedding, NVDD_PSI	NVDD_PSI	(5.1K pull High)
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K pull down)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K pull down)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K pull High)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF	(10K pull down)
GPIO11	OUT	LCD_VCC	LCD Panel VOLTAGE	GPU_EDP_ENVDD	(10K pull down)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K pull High)
GPIO13	OUT	UNUSED	UNUSED	UNUSED	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K pull High)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	UNUSED	
GPIO16	OUT	UNUSED	UNUSED	UNUSED	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_ENBKL	(100K pull down)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	IFPE_HPD	(10K pull High)
GPIO19	OUT	Reserved	UNUSED	UNUSED	
GPIO20	OUT	GC6:NB_FGC6	Low Power States Fast CG6	NB_FGC6	(10K pull down)
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	
GPIO22		UNUSED	UNUSED	UNUSED	
GPIO23		UNUSED	UNUSED	RASTER_SYNC1	(100K pull down)
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K pull High)
GPIO26		FP_FUSE	Field-programming of select fuses	GPIO26_FP_FUSE	(10K pull down)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K pull High)
GPIO28		ADC_MUX_SEL	OVRM MUX SEL	ADC_MUX_SEL_R	(10K pull High)
GPIO29	OUT	IDLE_IN_SW	IDLE_IN_SW	IDLE_IN_SW	(10K pull down)
GPIO30		UNUSED	UNUSED	UNUSED	

N18E-G1 Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.

2. Delay from 1V8_MAIN_EN to PEXVDD/NVDD_PGOOD must NOT exceed 45u.

3. It is recommended that the delay from 1V8_AON on to PEXVDD/NVDD_PGOOD assertion not exceed 20ms.

4. Power up NVDD must be 90% before PEXVDD can start ramp-up.

5. All 3.3V devices that connect to the GPU must be powered after 1V8_AON;GPU cannot have any 3.3V leakage path before 1V8_AON is present.

6. Refer to the JEDEC Memory SPEC for memory-related power sequencing.

7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6
1. PEXVDD must power down before NVDD,

2. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed

3. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

4. Power down of PEXVDD must be less than 10% before NVDD can start ramp-down..

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

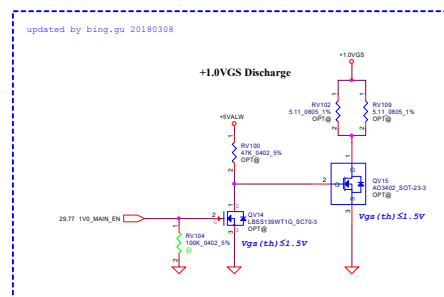
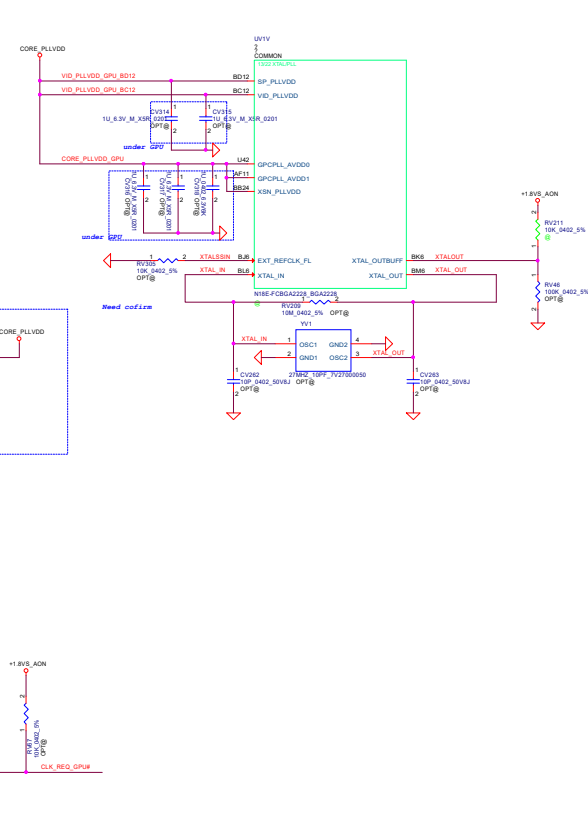
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	N18E-G1 VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	


FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	L	FS_OVERT# function ENABLE
L	L	H	FS_OVERT# function DISABLED Reserved; do not configure

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

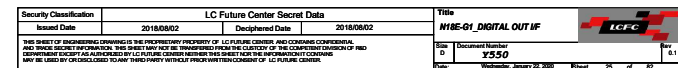
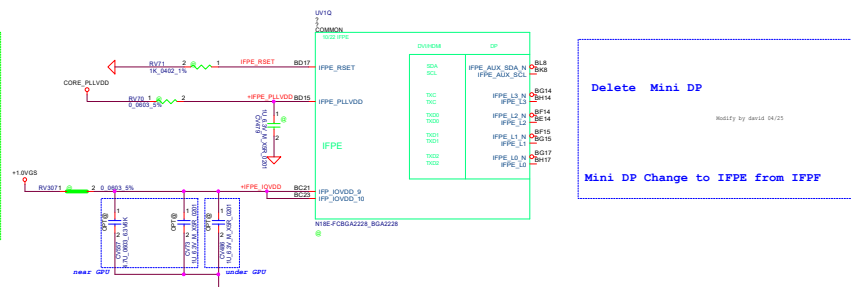
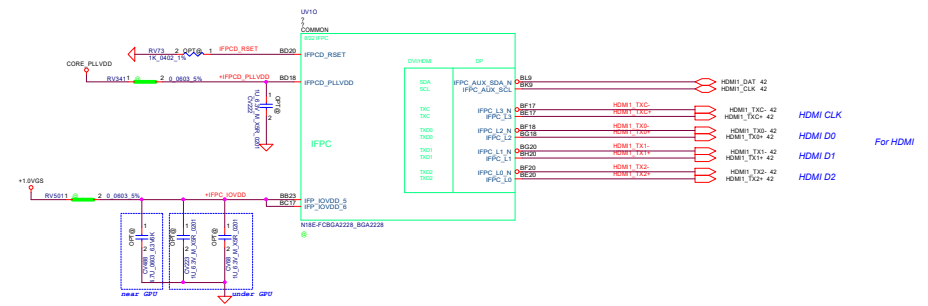
- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

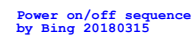


Security Classification	LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	

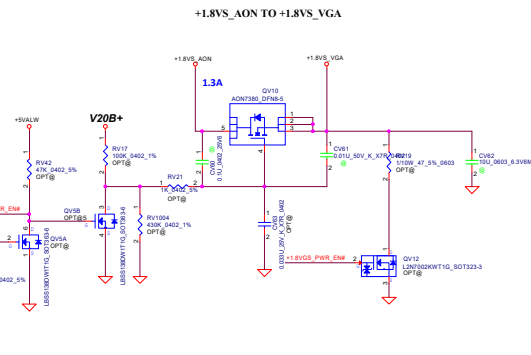
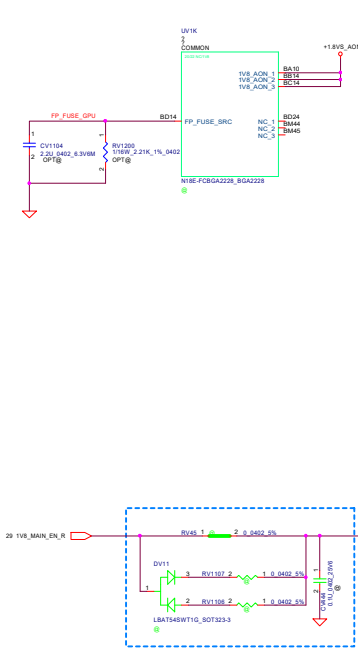
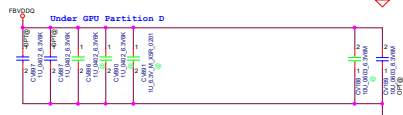
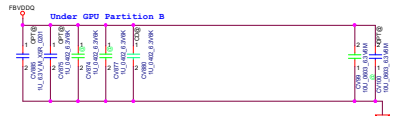
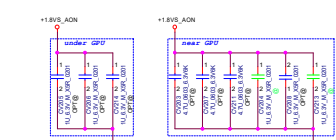
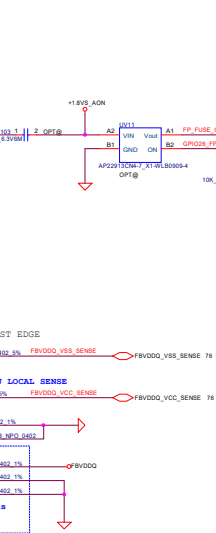
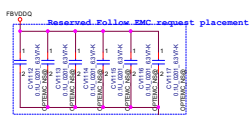
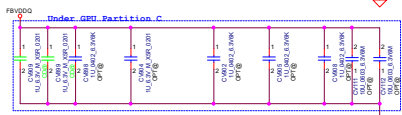
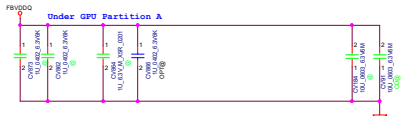
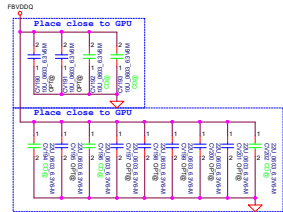
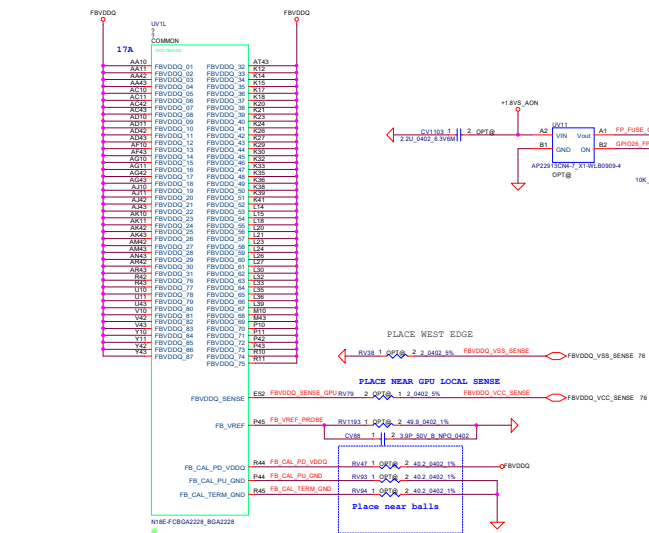
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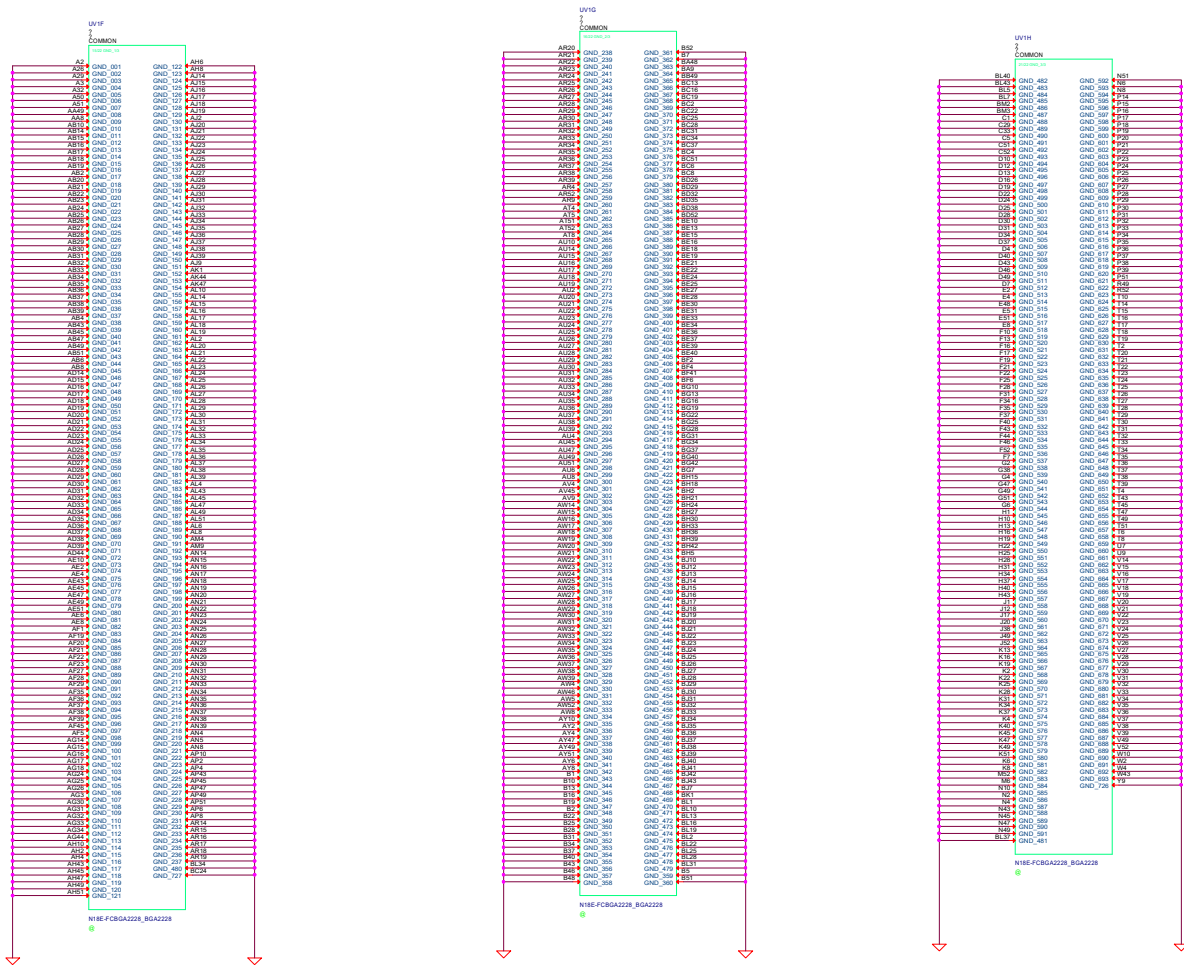


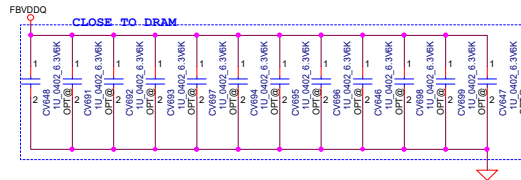
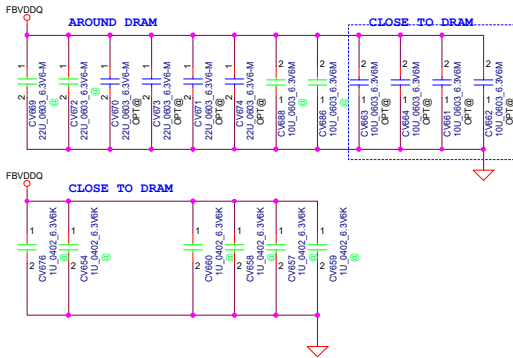
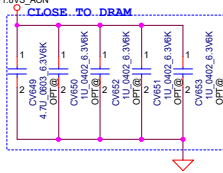
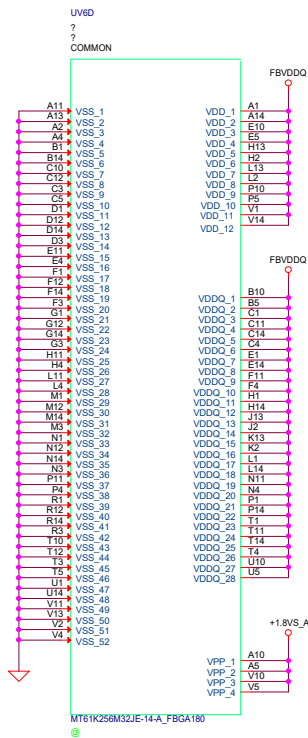


	N18E-G3	N18E-G2	N18E-G1
Product Part Number	N18E-G3-A1	N18E-G2-A1	N18E-G1-KD-A1
NVIDIA Part Number ¹ (used on labels of packaging materials)	TU104-750-A1	TU106-750-A1	TU106-725-KD-A1
Device ID	<ul style="list-style-type: none"> Primary: 0x1E90 Secondary: 0x1ED0 	<ul style="list-style-type: none"> Primary: 0x1F10 Secondary: 0x1F50 	<ul style="list-style-type: none"> Primary: 0x1F11 Secondary: 0x1F51
Memory interface	256-bit GDDR6	256-bit GDDR6	192-bit GDDR6
Package	GB4B-256	GB4B-256	GB4B-256

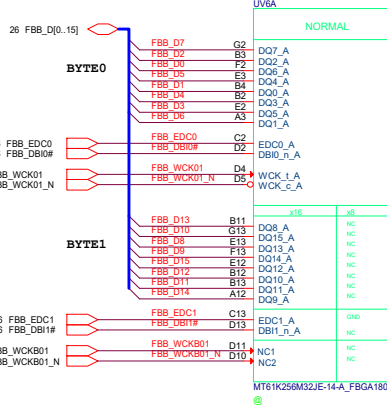


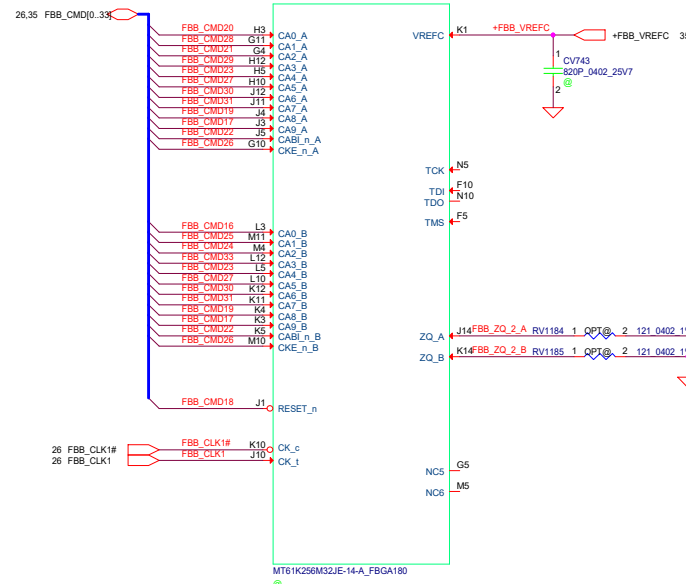
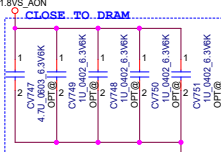
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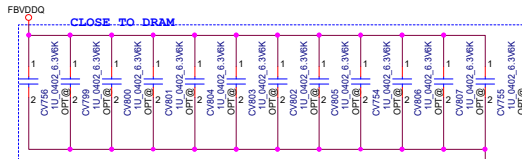
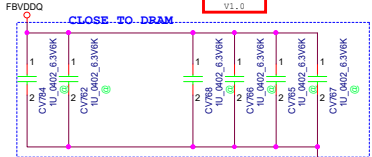
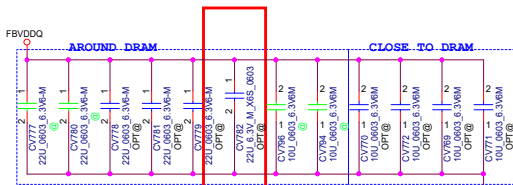
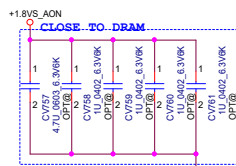
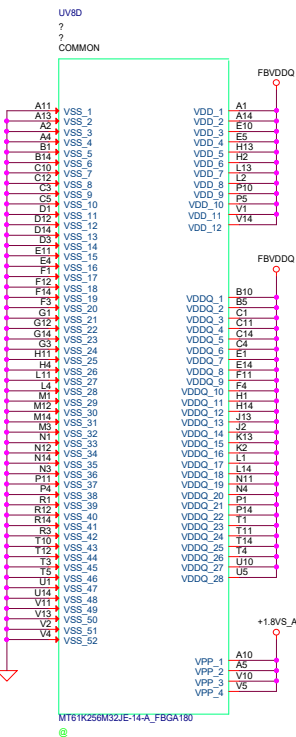




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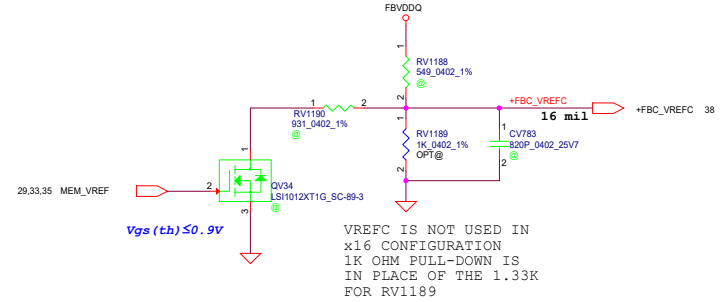
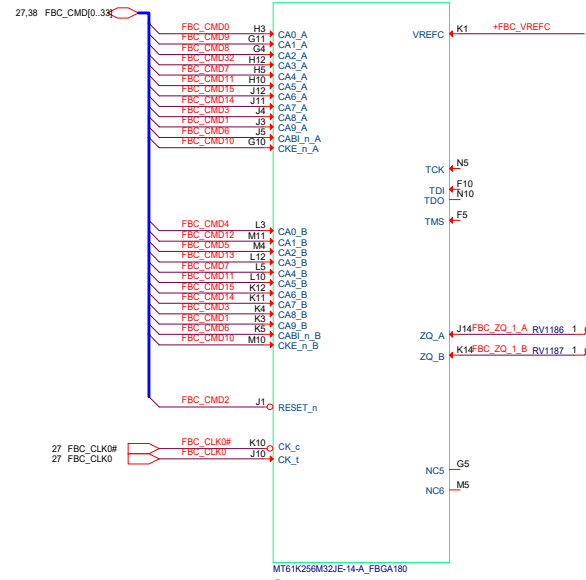
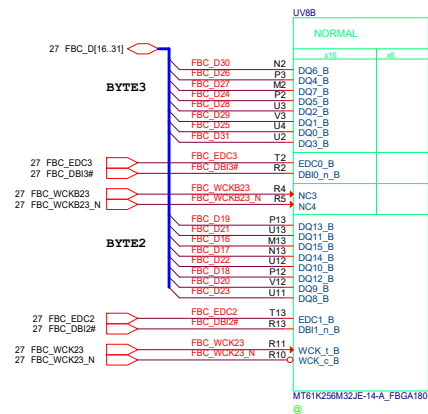


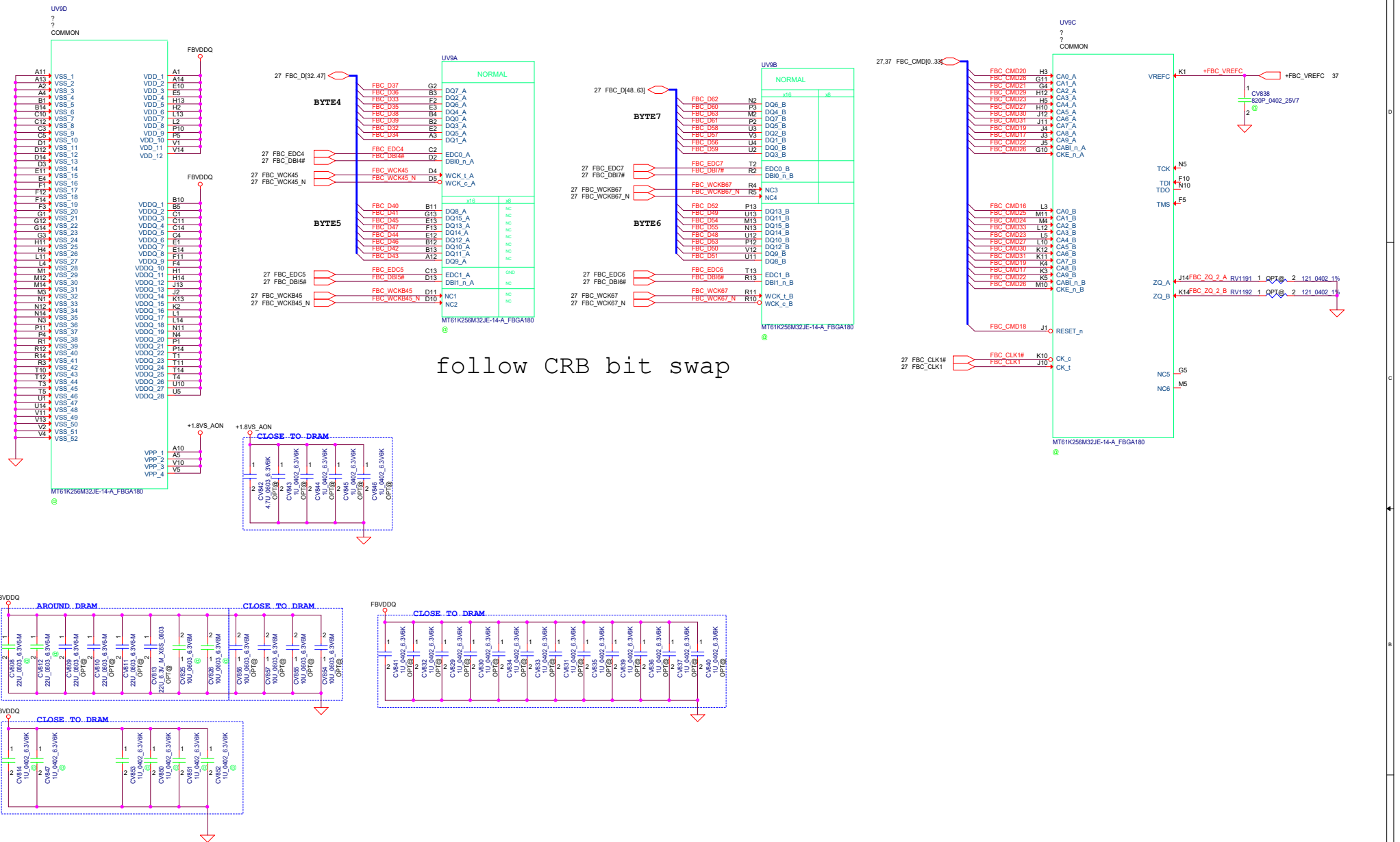


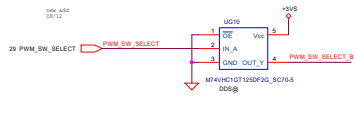


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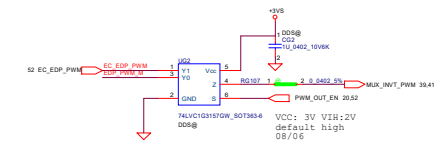
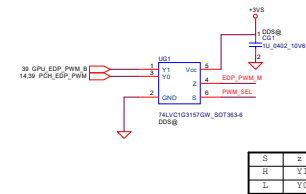
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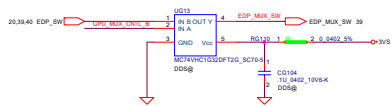
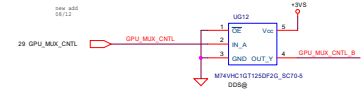




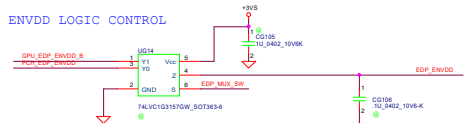
EDP PWM LOGIC CONTROL



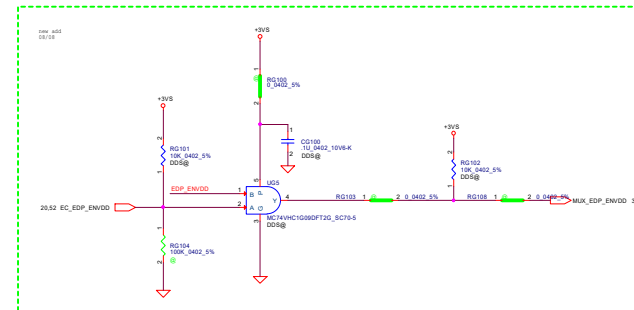
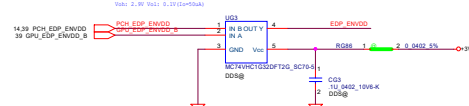
S	Z
H	Y1
L	Y0



Co-lay EDP ENVDD LOGIC CONTROL



EDP ENVDD LOGIC CONTROL



level shift for I2C

EDP backlight LOGIC CONTROL

VIN: 2.1V VOUT: 0.9V
VIN: 2.1V VOUT: 0.9V (VIN=VOUT)

14.39 PCH_EDP_ENBLK
39 GPU_EDP_ENBLK_B

29 GPU_EDP_ENBLK

29 GPU_EDP_ENBLK

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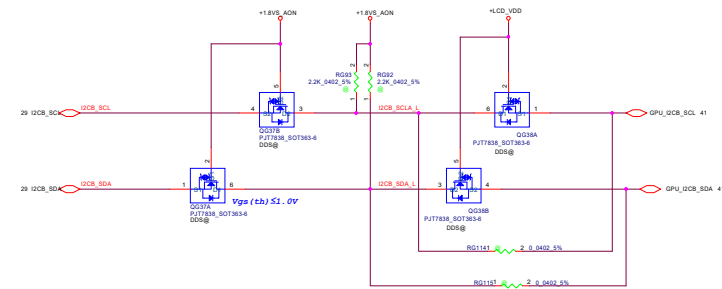
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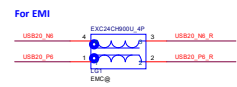
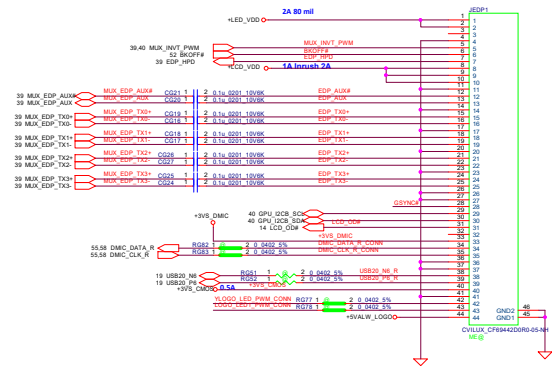
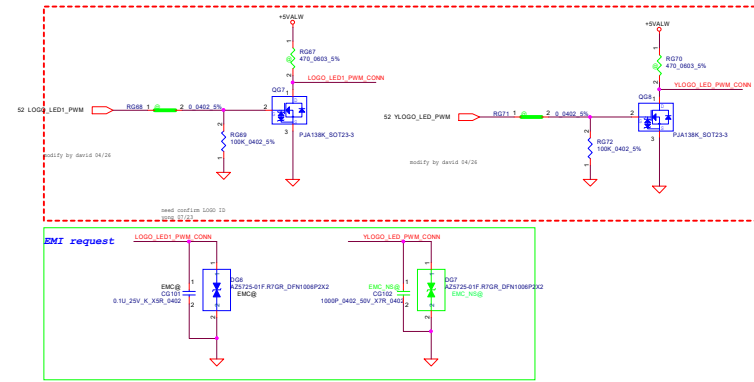
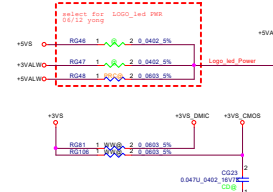
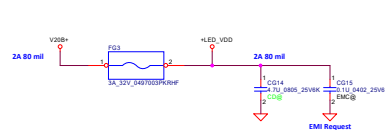
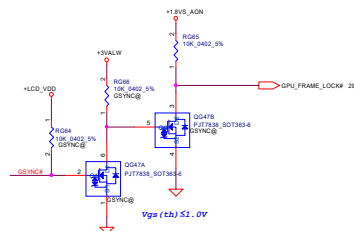
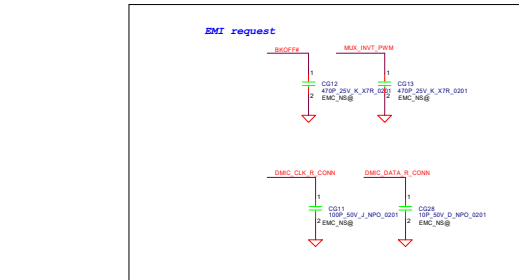
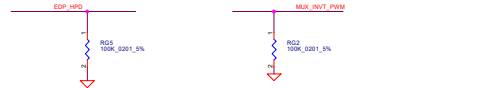
29 GPU_EDP_ENBLK

29 GPU_EDP_ENBLK

29 GPU_EDP_ENBLK

29 GPU_EDP_ENBLK



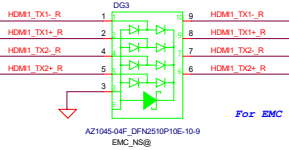
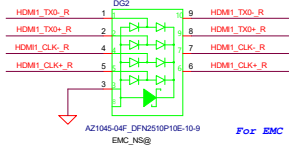
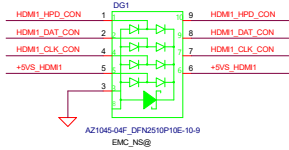
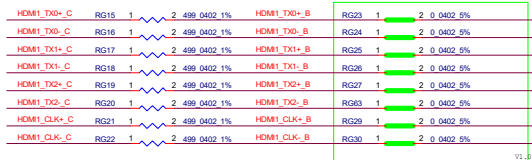


HDMI D0

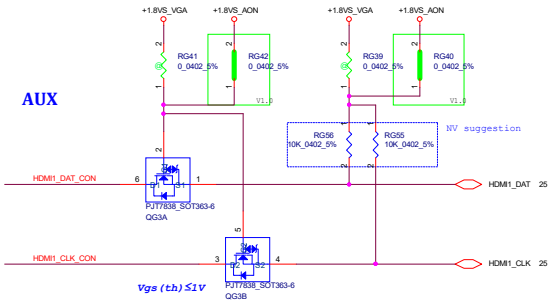
HDMI D1

HDMI D2

HDMI CLK



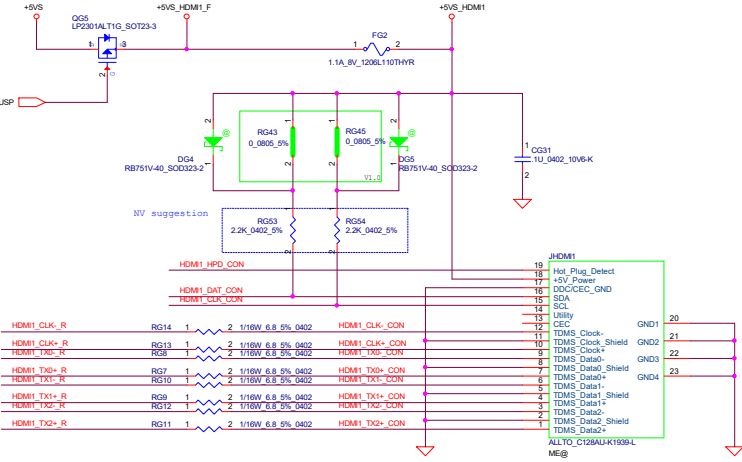
AUX



update by bing
20180316

29 IFPC_HPD

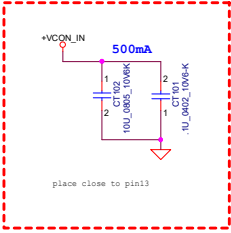
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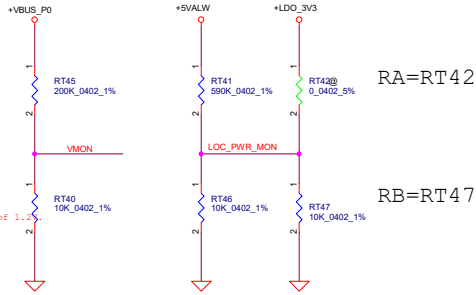
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	Document Number	Y550
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Date:	Wednesday, January 22, 2020	Sheet	42	of	83

Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K

VMON:
Used to monitor VBUS voltage.
Divide the VBUS voltage down to ADC full-scale input of 1.2V.
Then connect the divided voltage to this pin.

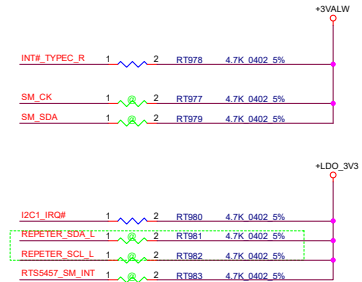
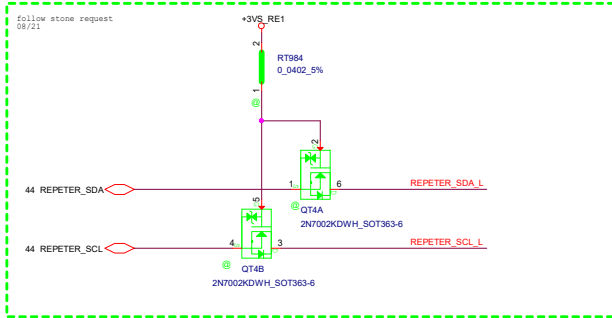
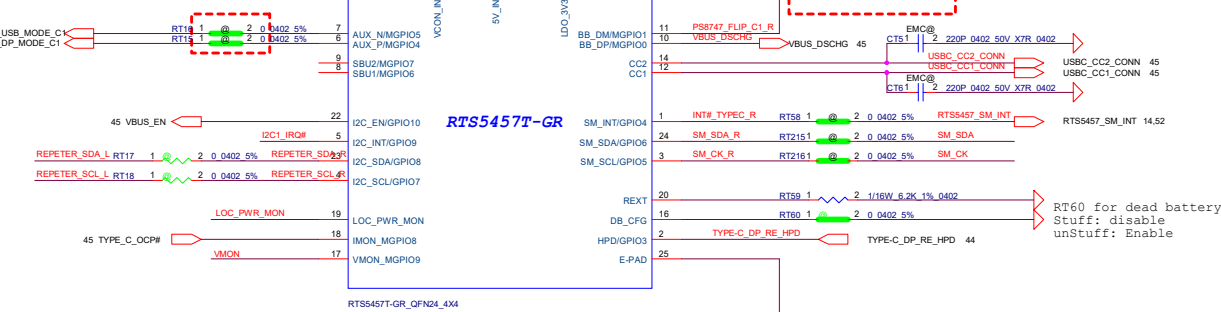
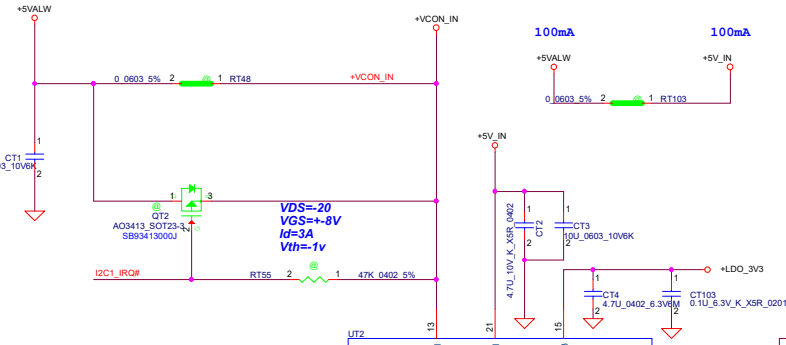
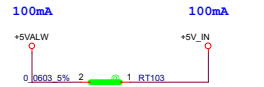
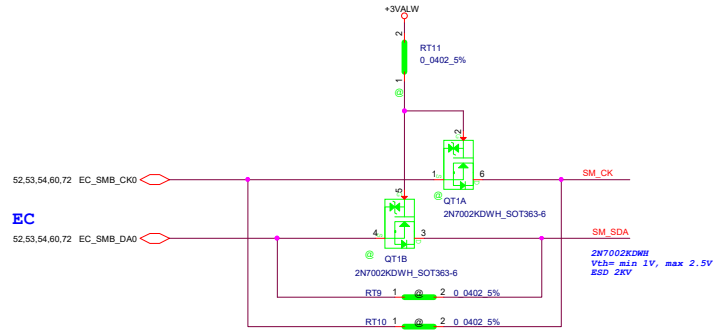


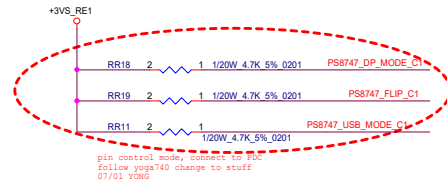
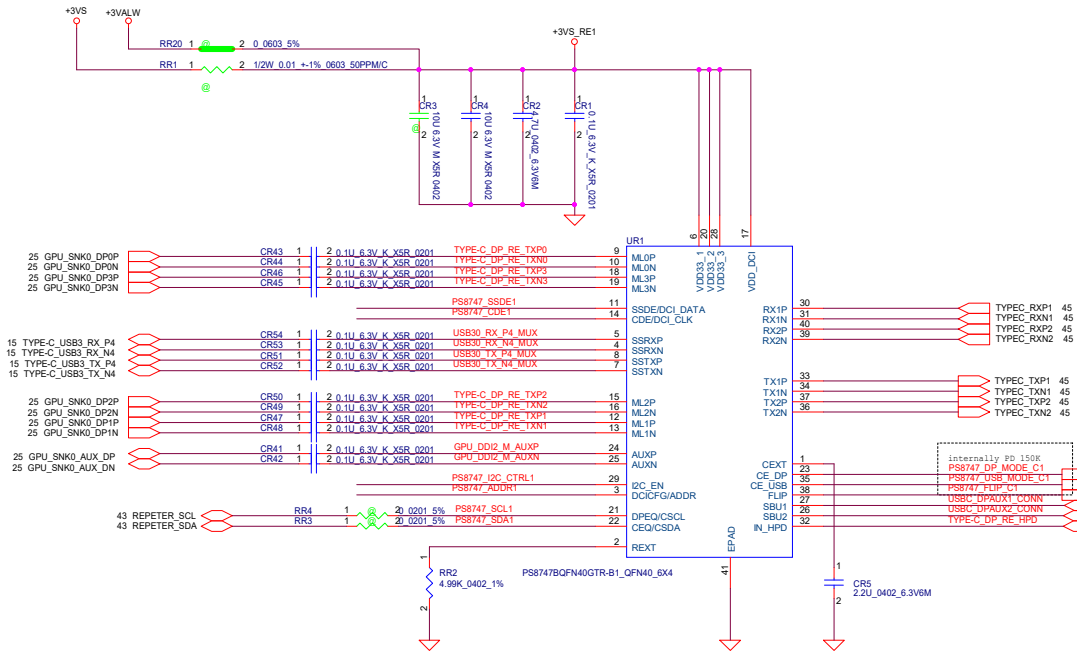
for redriver pin control mode used
06/13 yong



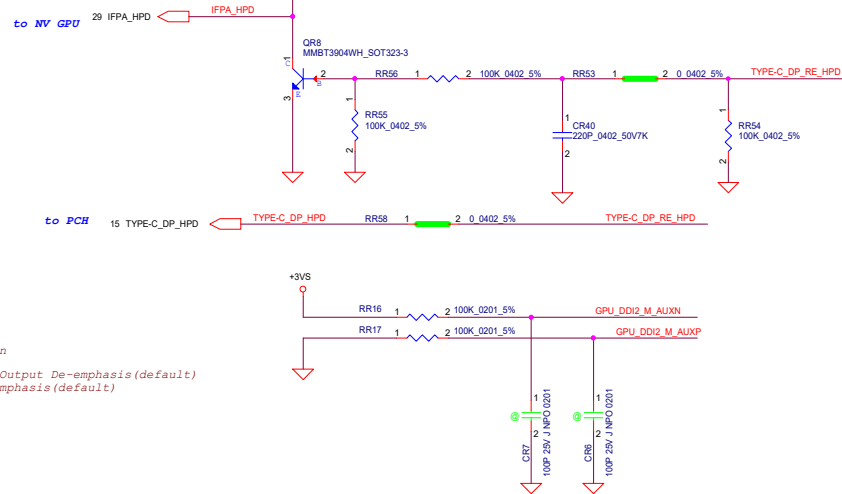
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RB=RT47

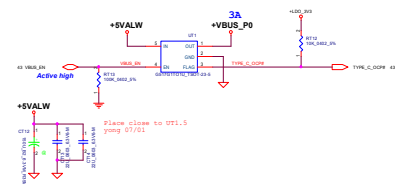
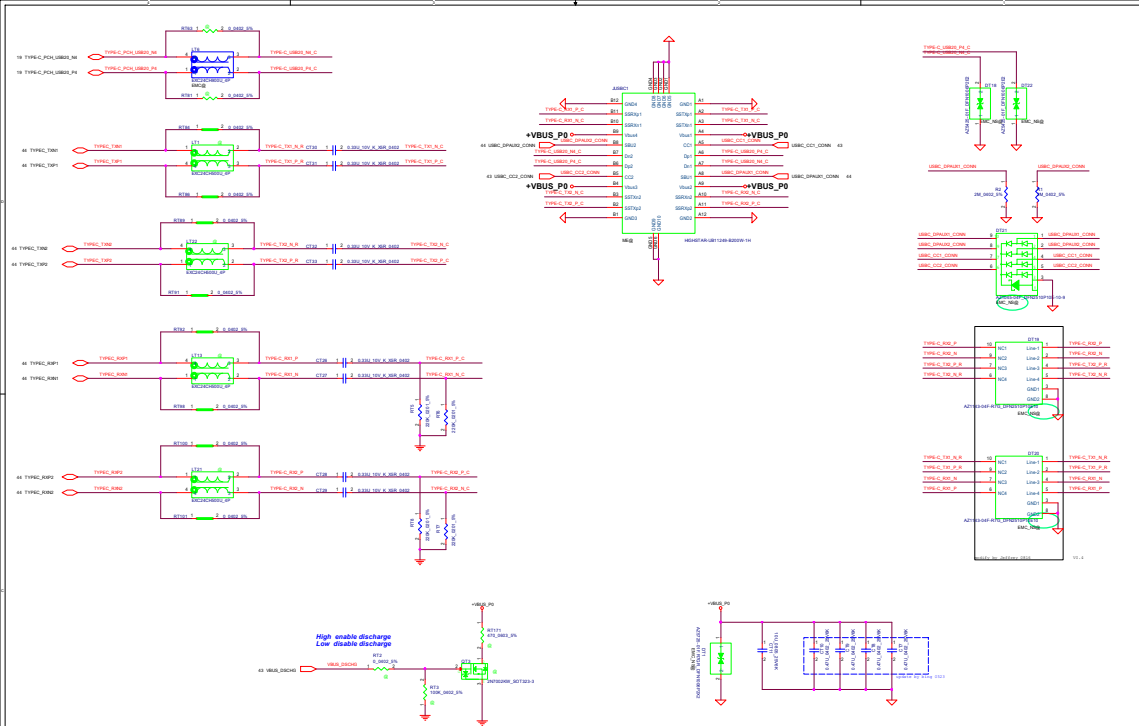




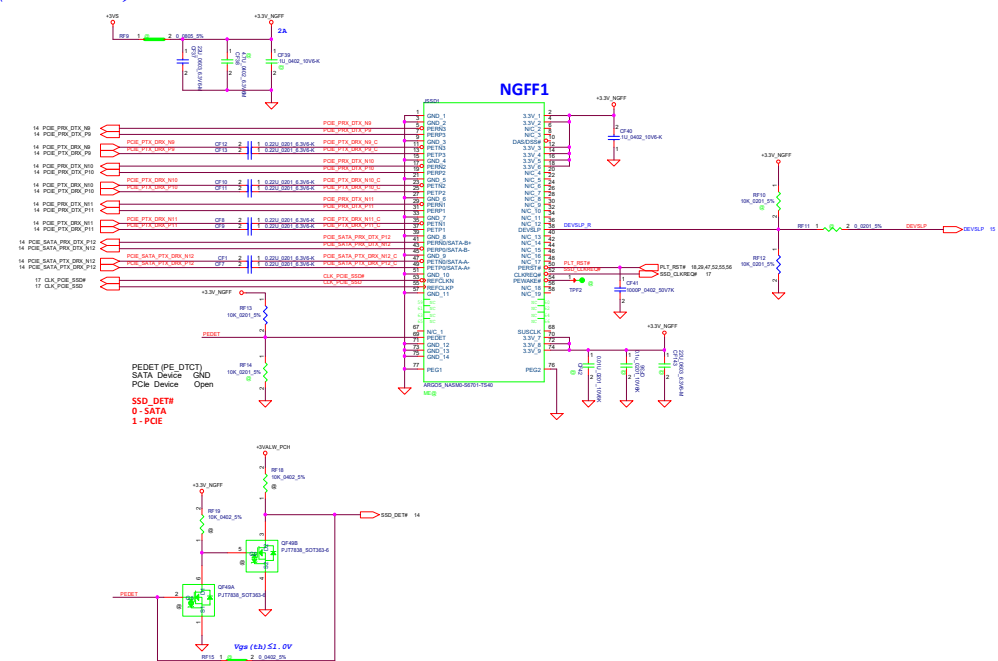
HPD



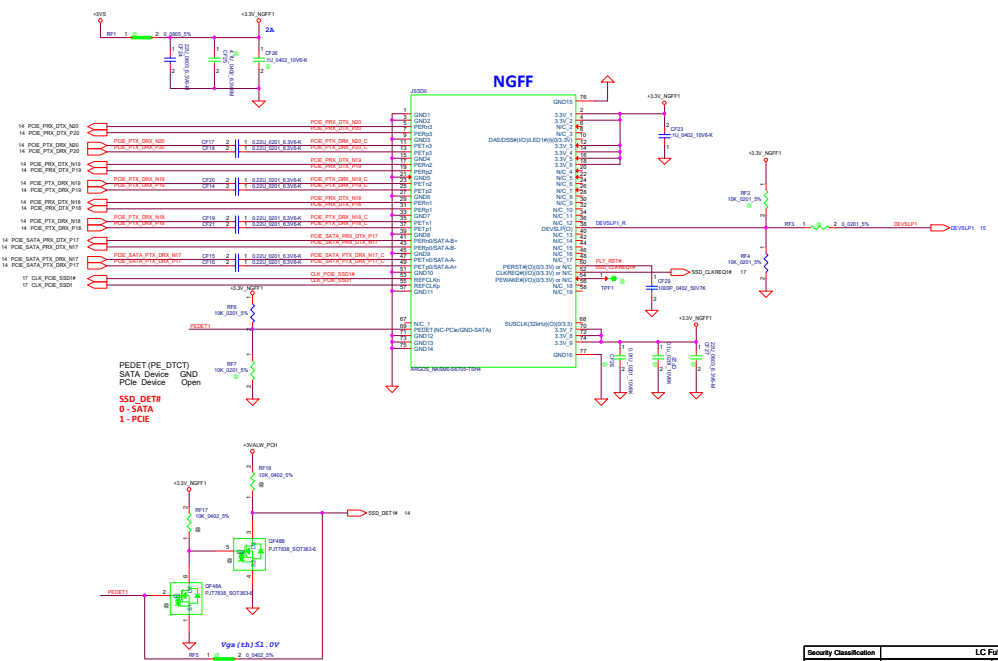
Setting:
 1. PS8747_I2C_CTRL=L, I2C disable
 2. PS8747_SCL/DPEQ=L, DP Receiver equalization Compensation for channel loss up to 7dB
 3. PS8747_SDA/CEQ=L, USB Type-C connector facing RX channel receiver equalization setting Compensation
 4. ADDR/DCICFG=M, Automatic DCI mode entering enabled for channel loss up to 7dB
 5. CDE/DCICLK=L, When NO DCI mode-->USB Type-C connector facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)
 6. SSDE/DCIDAT=L, When NO DCI mode-->USB HOST facing TX channel De-emphasis setting -3.5dB Output De-emphasis(default)



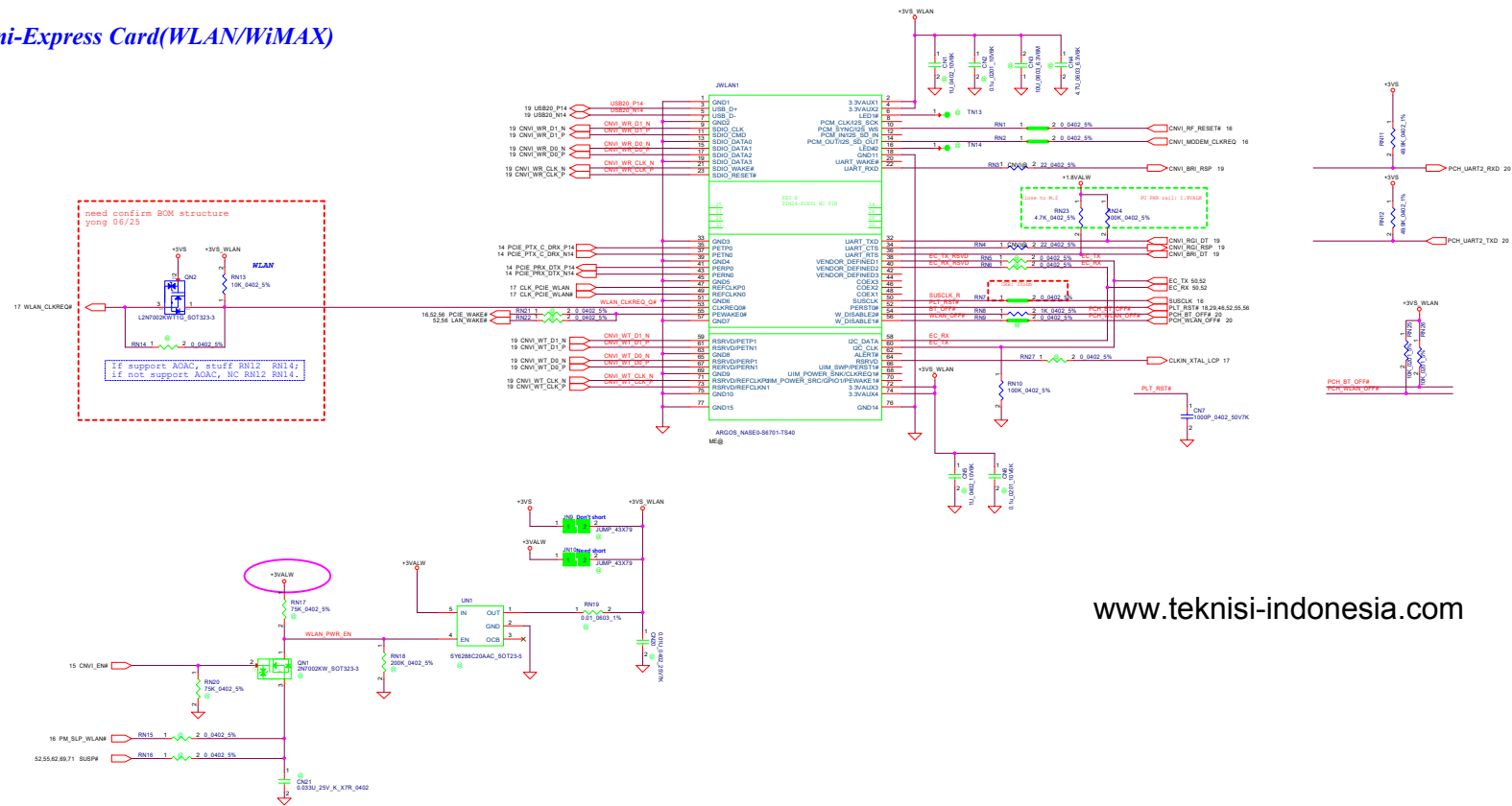
M.2 SSD(SATA/PCIE)






M.2 SSD(SATA/PCIE)



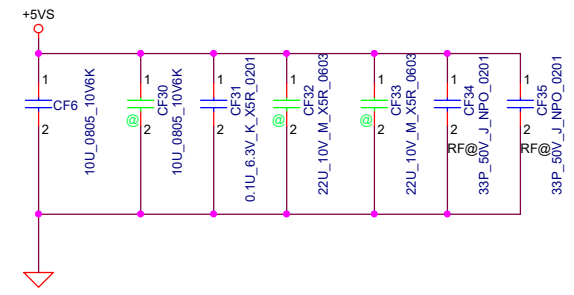
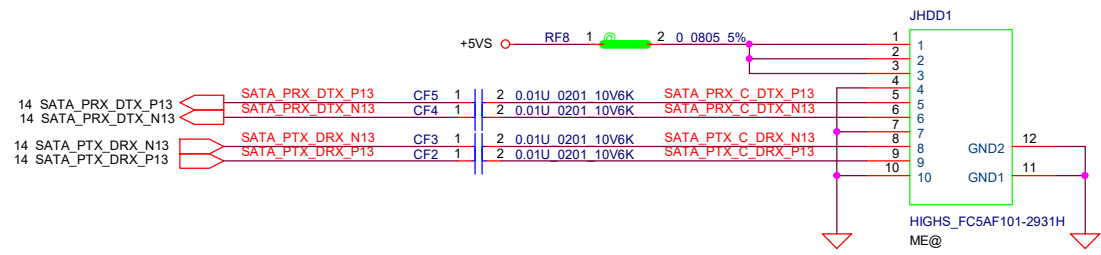
Mini-Express Card(WLAN/WiMAX)




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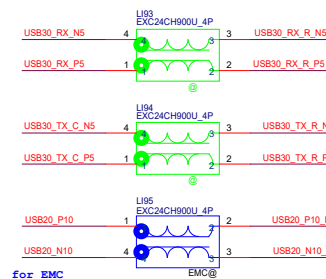
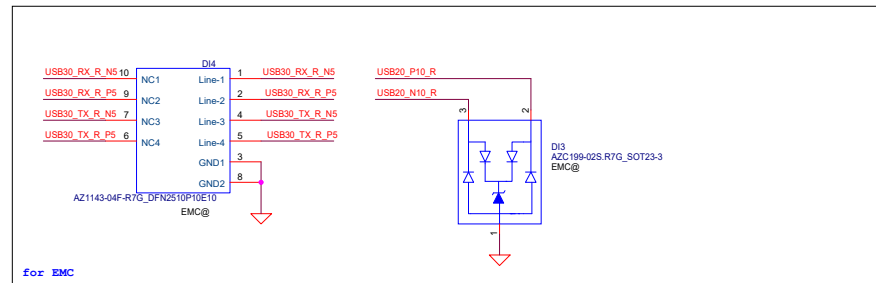
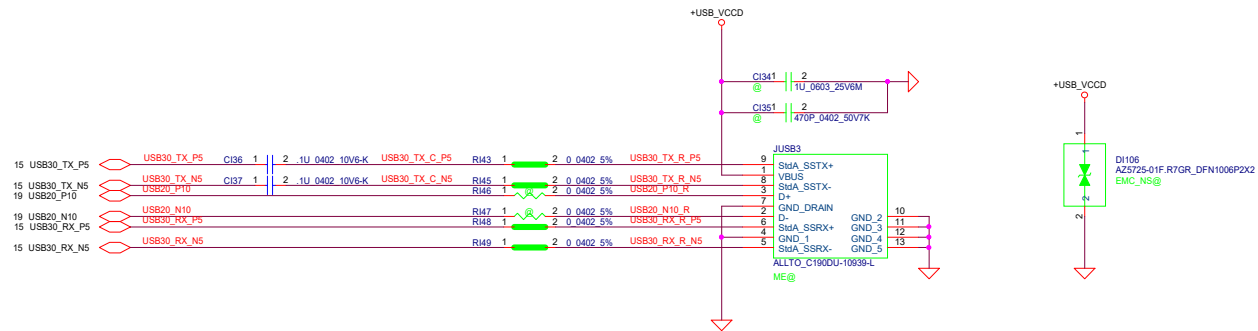
Security Classification	LC Future Center Secret Data		Title	 	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Doc#	Decipherment Number
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			Documenting: January 29, 2003	Sheet	47 of 53

SATA HDD Conn.



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Issued Date		2018/08/02		Deciphered Date		2018/08/02			
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Size		Document Number				Rev			
B		Y550				0.3			
Date:		Wednesday, January 22, 2020		Sheet		48		of 83	





For EMI

For SPI ROM Mirror

Close EC

minimum trace width 12 mil

Reserved Cap HLZ SDV 0616

ITE-IT8227E-192/CX LQFP128

SA00009CZ20 support ECC function

Change RE30 to 0ohm jump

For factory EC flash

same net name with PCH

when mirror, GP2 pull high when no mirror, GP2 pull low

Security Classification

LC Future Center Secret Data

Title

Issued Date

Deciphered Date

Size

Document Number

Y550

Date

Monday, February 10, 2020

Sheet

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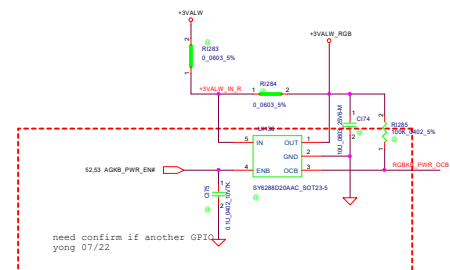
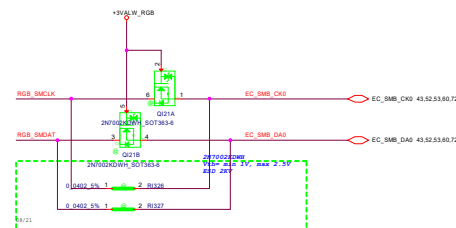
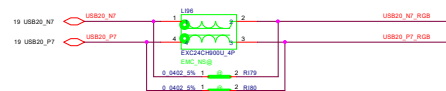
Rev

0.3

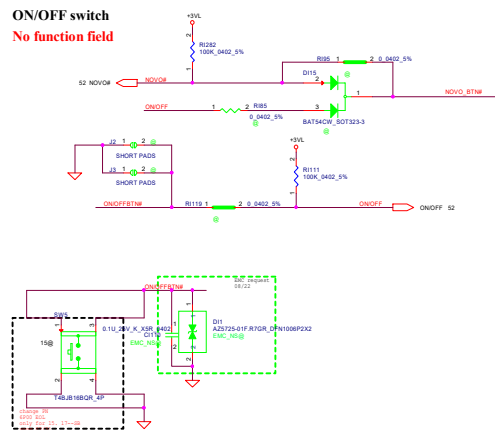
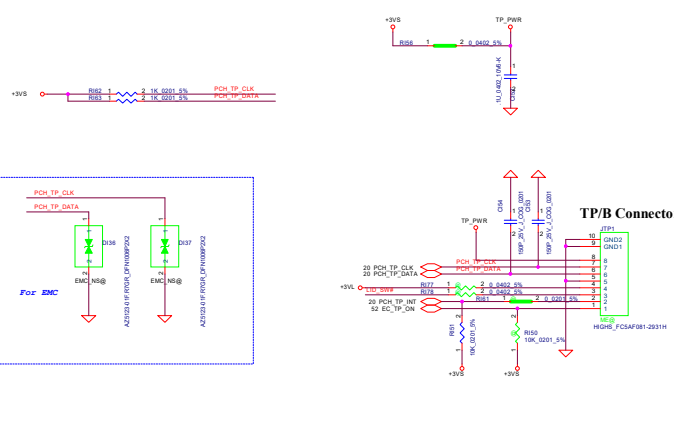
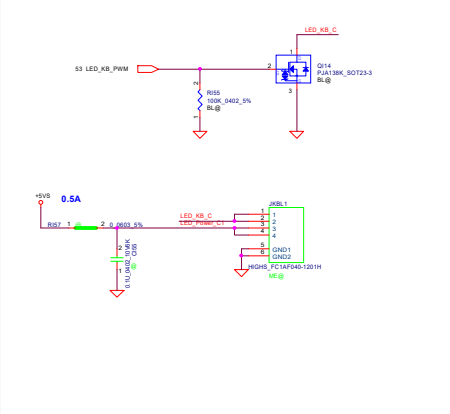
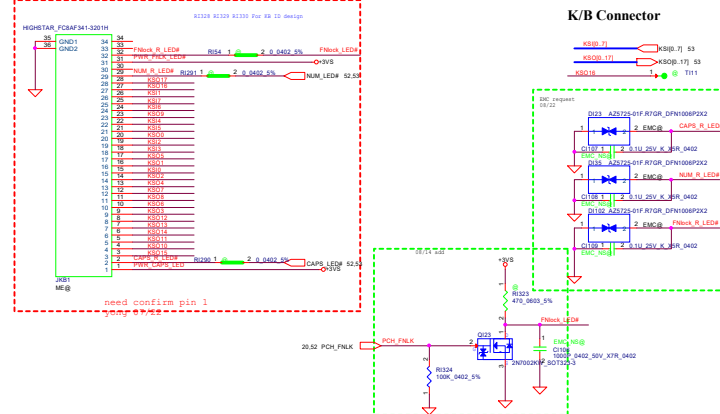
ICFC

Rev

0.3



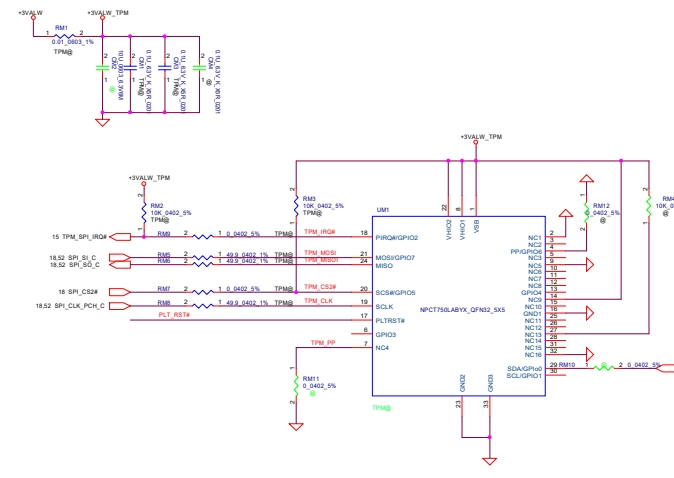
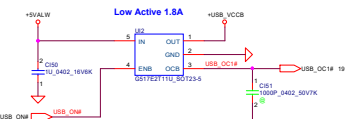
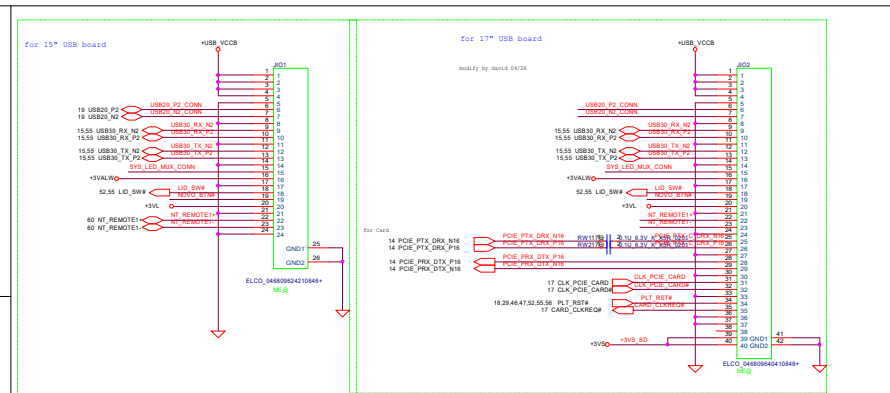
No function field


[illegible]

PWR LED

The schematic diagram illustrates the PWR LED circuit. It features three main output pins: PWR_LED_PWM_B OUT, PWR_LED_PWM_G OUT, and PWR_LED_PWM_R OUT. Each output pin is connected to a 10K resistor (R232, R233, R234) and a 100K resistor (R235, R236, R237). The circuit is powered by a 5V supply (V5) and a 5V supply (V5). The circuit includes a 10K resistor (R232), a 100K resistor (R235), a 10K resistor (R233), a 100K resistor (R236), a 10K resistor (R234), a 100K resistor (R237), a 10K resistor (R238), and a 100K resistor (R239). The circuit also includes a 10K resistor (R232), a 100K resistor (R235), a 10K resistor (R233), a 100K resistor (R236), a 10K resistor (R234), a 100K resistor (R237), a 10K resistor (R238), and a 100K resistor (R239).

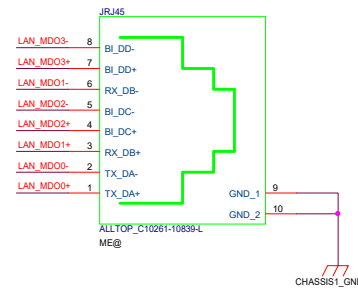
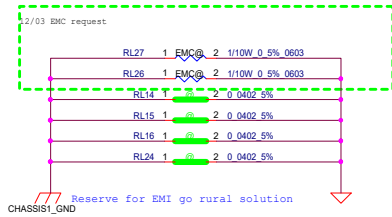
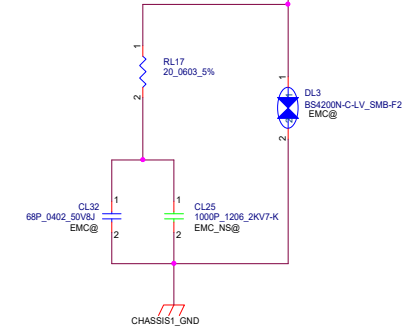
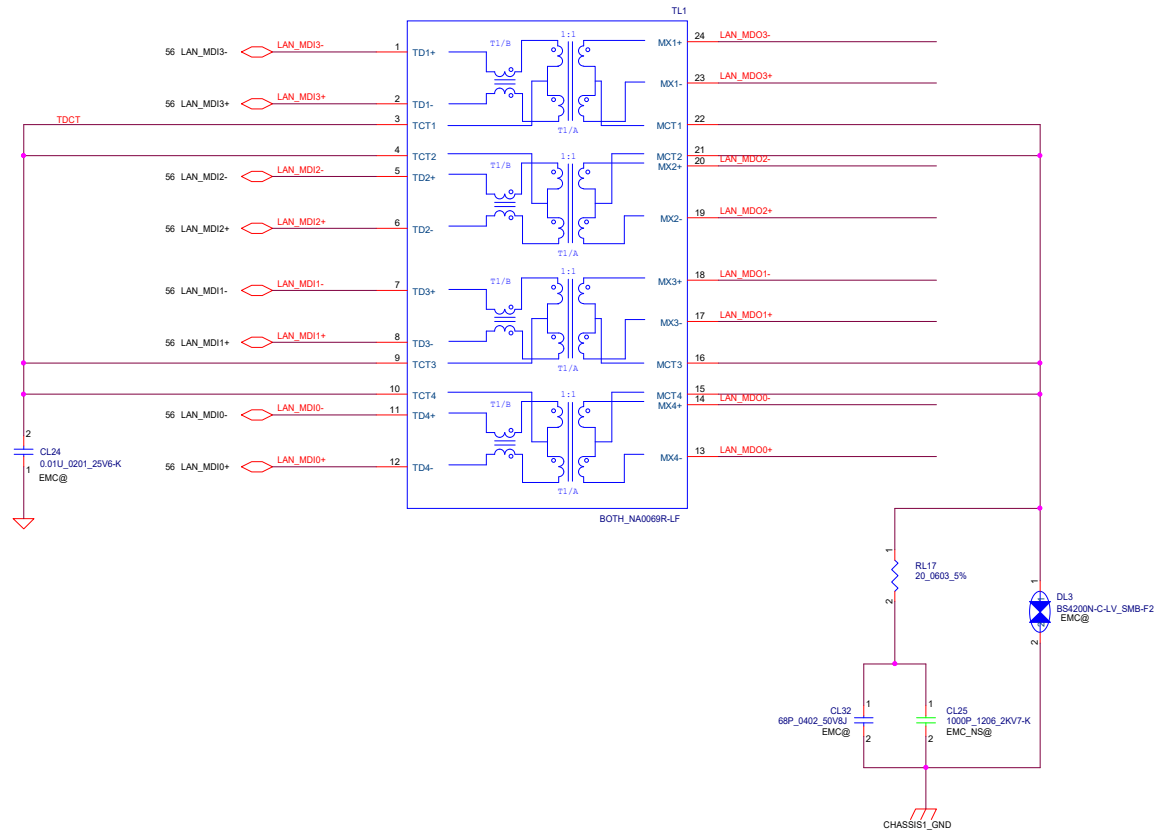
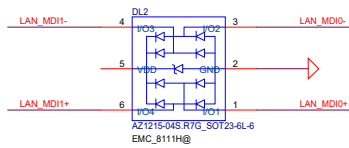
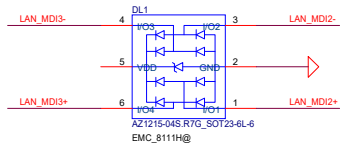
USB3.1 PORT x1

[illegible][illegible]

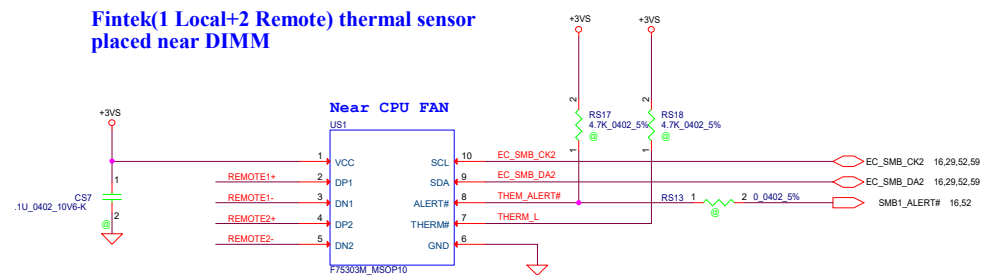
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	KBD/PWR/IO/LED/TP Conn.	
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DL1/DL2
1'S PN:SC300005900

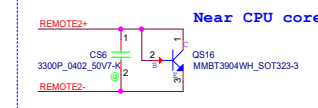
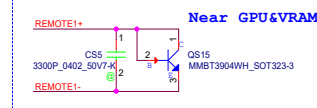
Place Close to TL1



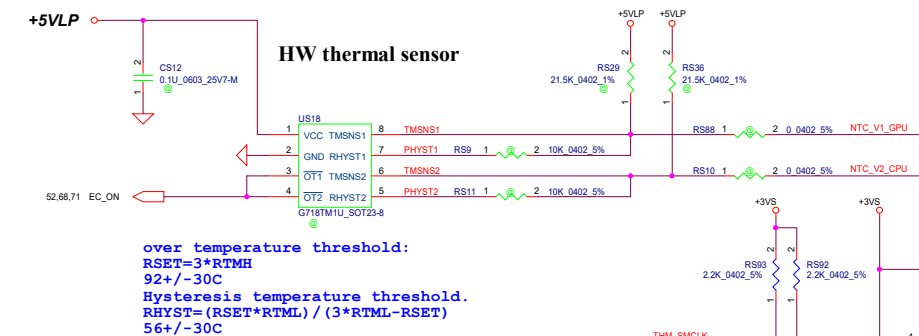
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM



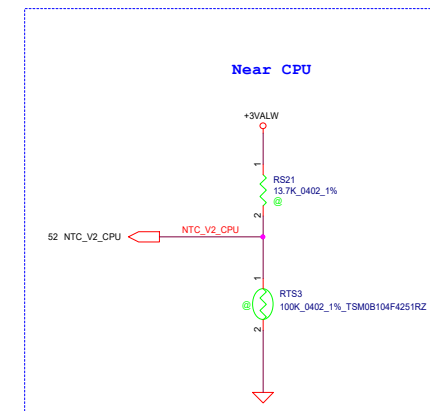
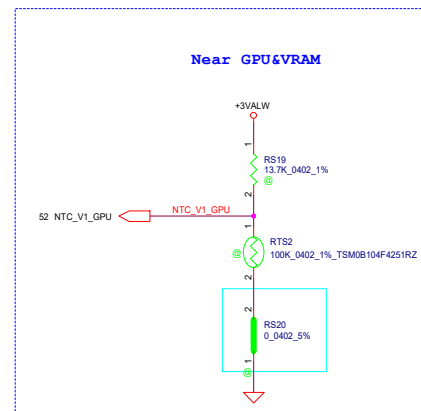
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



HW thermal sensor

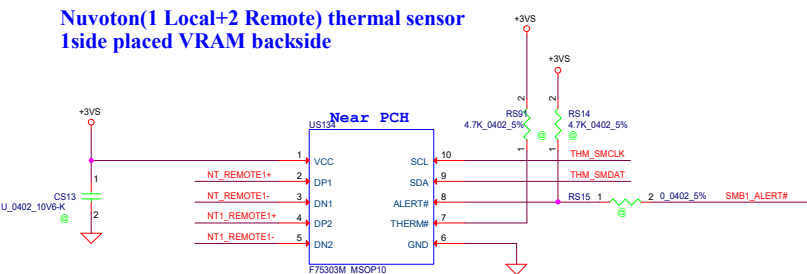


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML) / (3*RTML-RSET)
56+/-30C

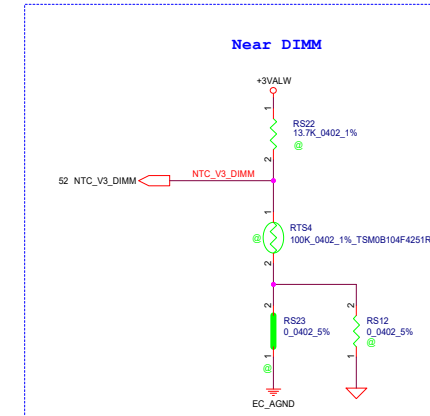
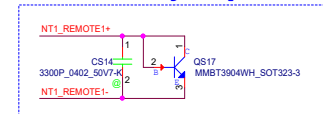


for layout optimized, change the EC_AGND to GND

Nuvoton(1 Local+2 Remote) thermal sensor 1side placed VRAM backside



Near VRAM high Temp side



Address 1001_101xb

FAN Conn Right

FAN Conn LEFT

NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

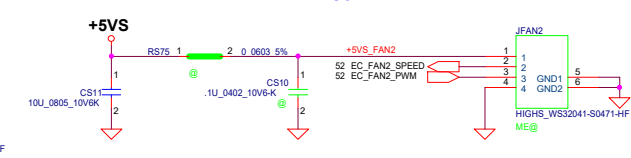
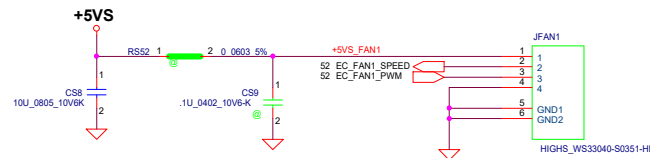




TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

↑
LOGIC

TABLE : PCH ITP DEBUG REPORT

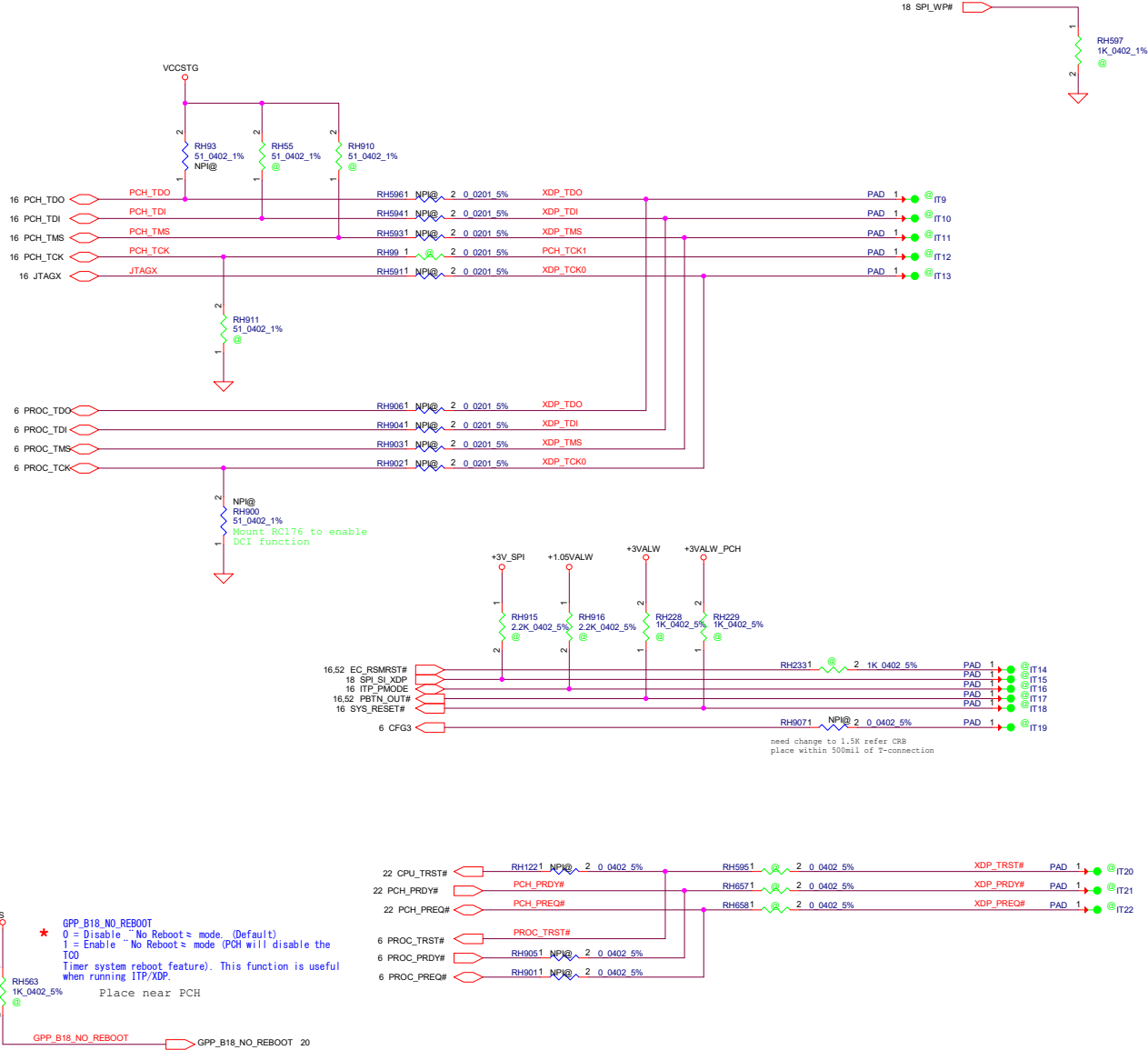
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

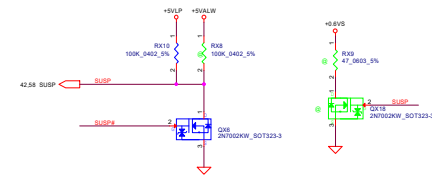
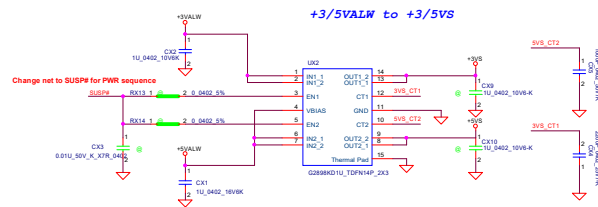
↑
LOGIC

TABLE : Functional Strap

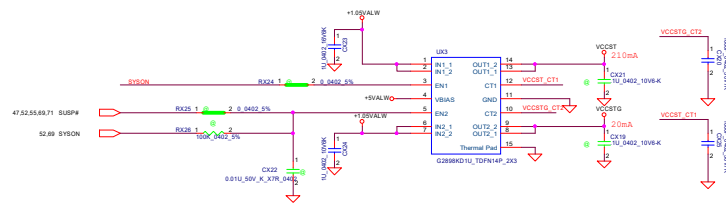
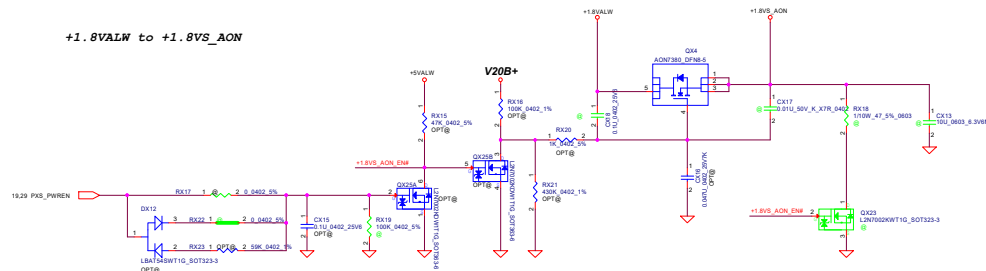
GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

← LOGIC

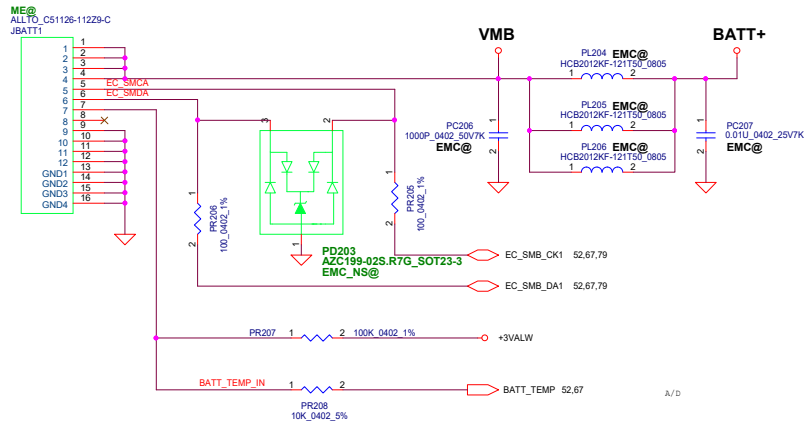
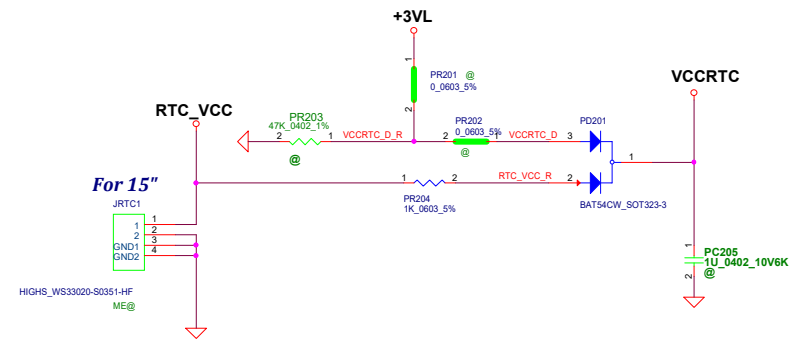
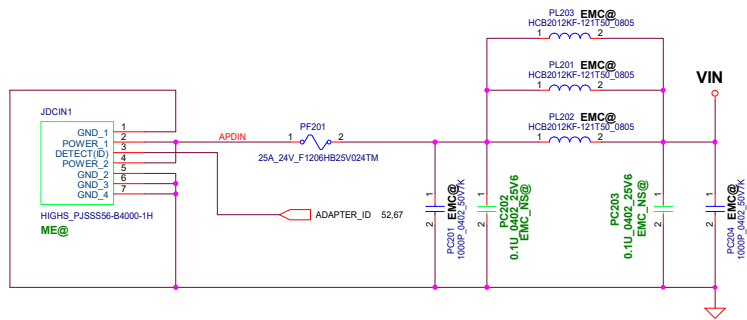




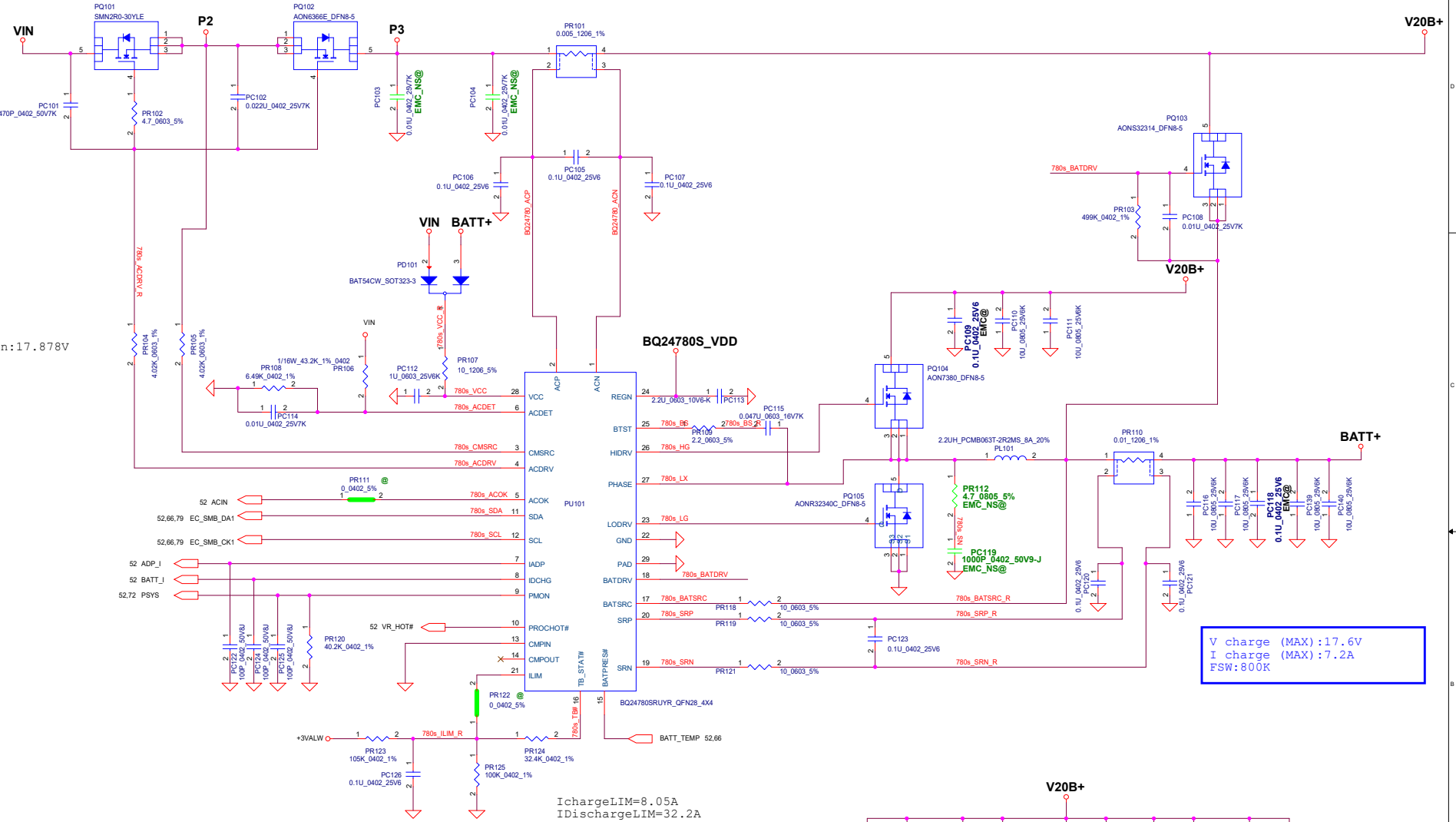
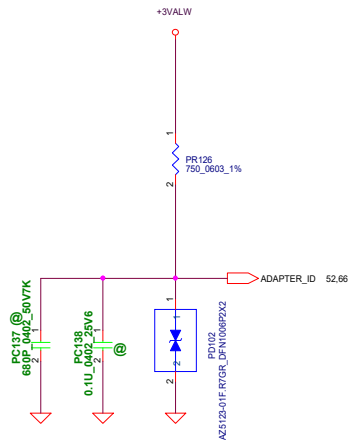
+1.8VALW to +1.8VS_AON



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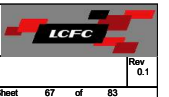


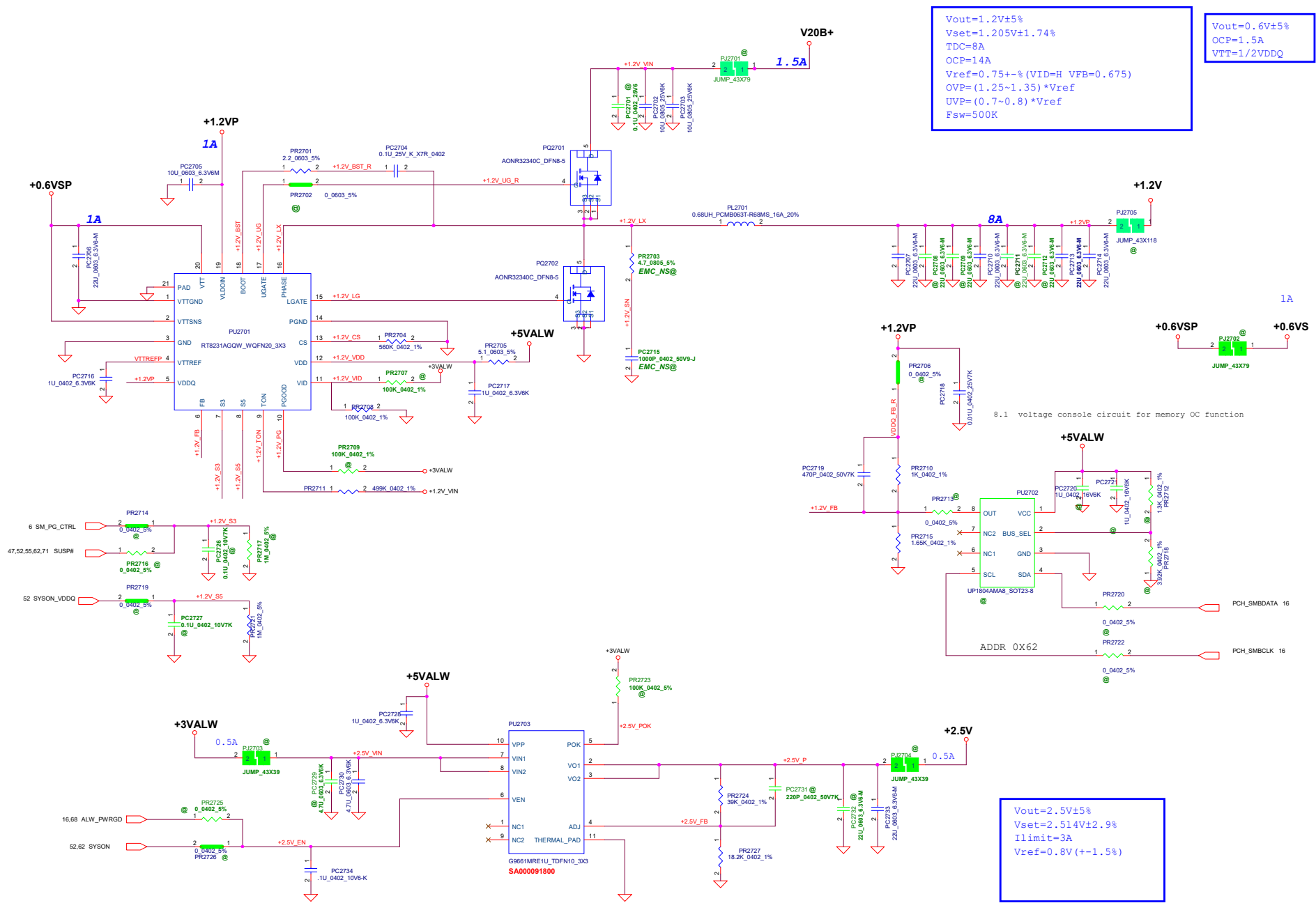
ACDET Threshold:min:17.878V
BAT Max V=17.6V



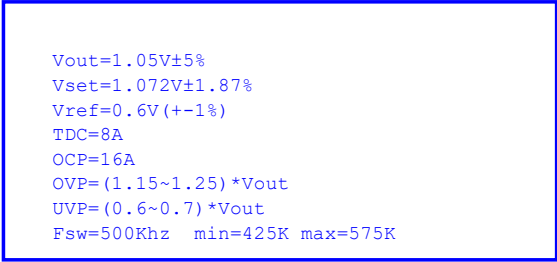
IchargeLIM=8.05A
IDischargeLIM=32.2A

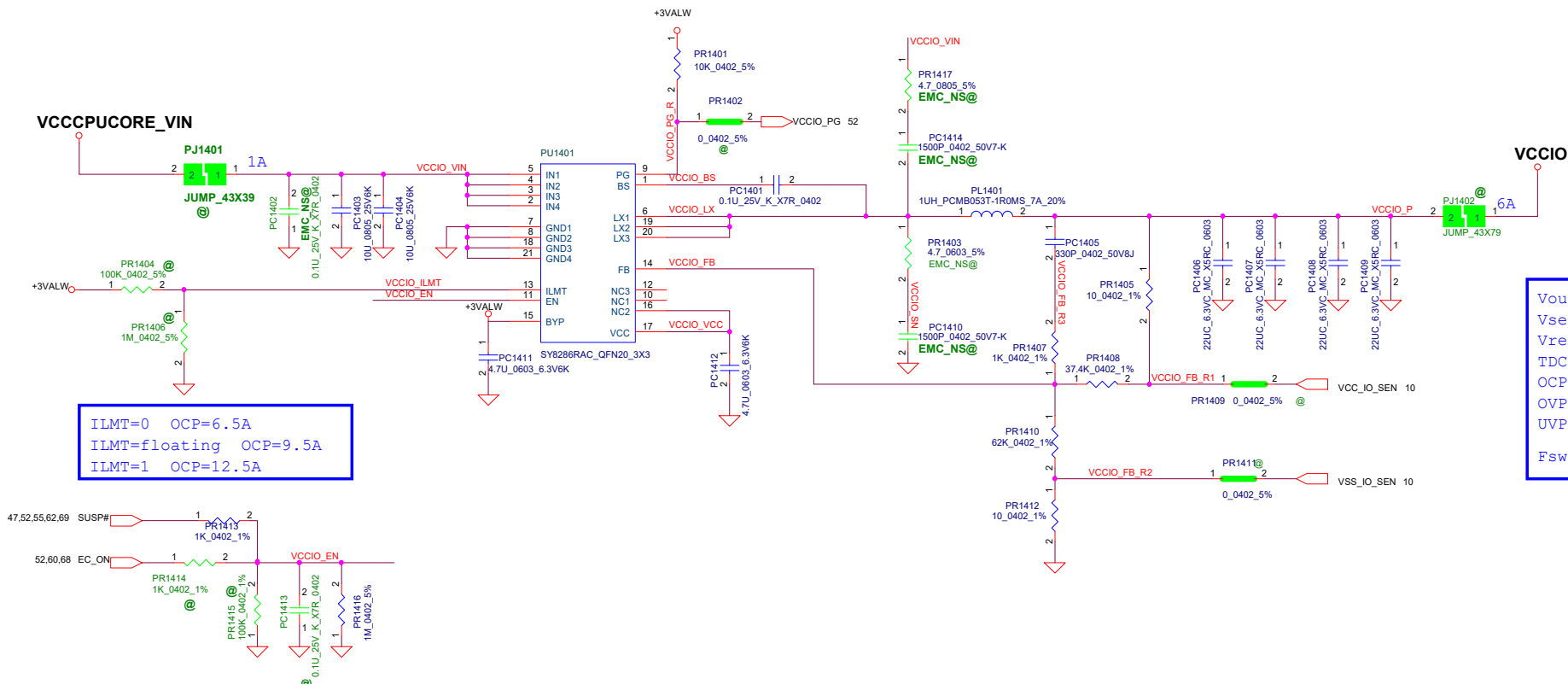
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR-charger	
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				Date Wednesday, January 29, 2020	Sheet 67 of 83






STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off



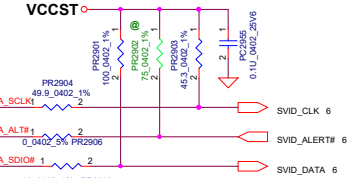



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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR-VCCIO	
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				Date: Wednesday, January 22, 2020	Sheet 71 of 83



Rev 0.1

PSYS=0.8V MP2949 trigger VRHOT



Security Classification	LC Future Center Secret Data			Title	
Issued Date	2016/01/20	Deciphered Date	2016/01/20	PWR-IMPV8_MP2949	
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Date: Wednesday, January 22, 2020					Sheet 72 of 83

Phase4 Phase5 Phase Double share CS4 PWM1
CS share CS4

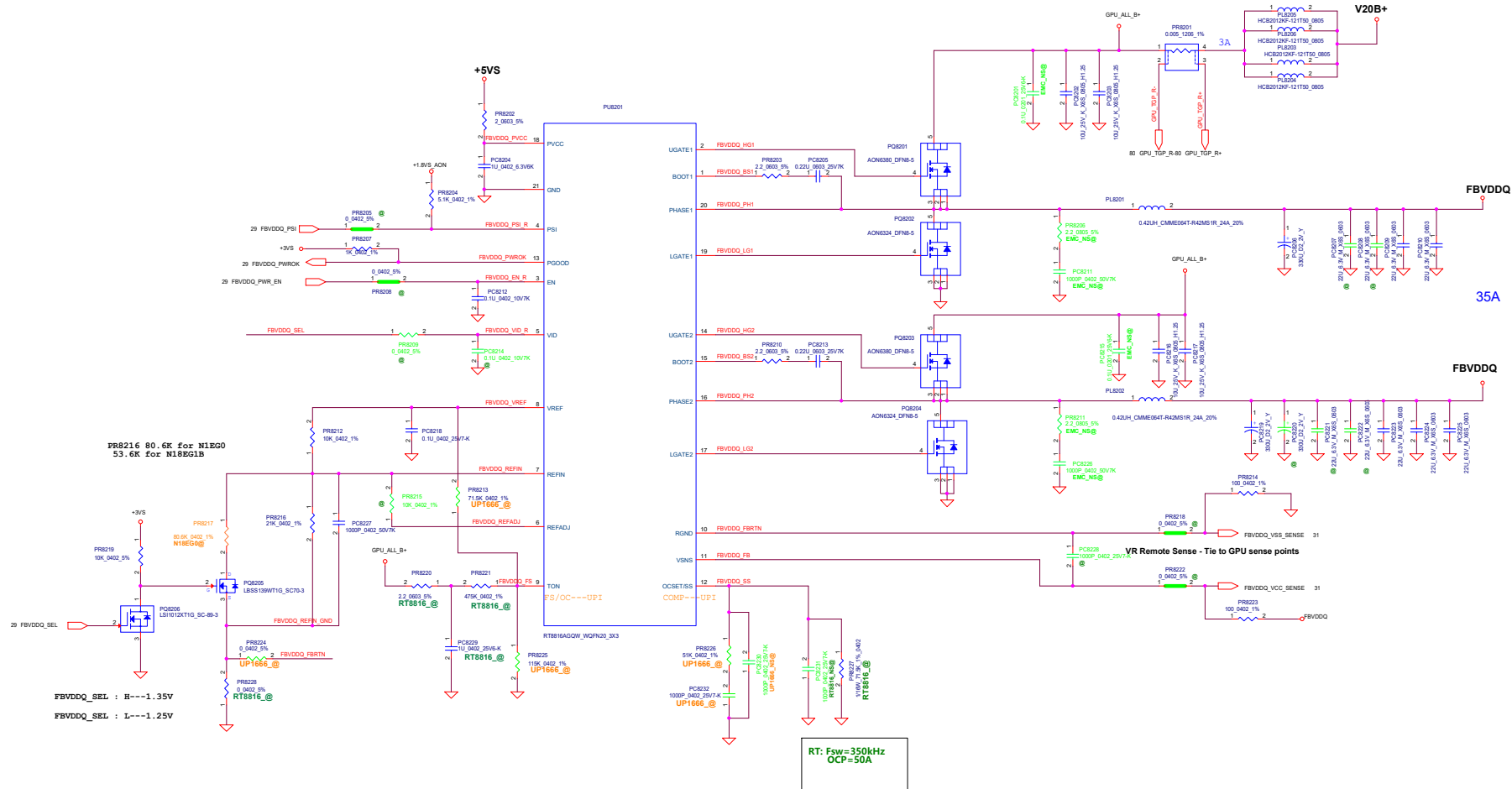
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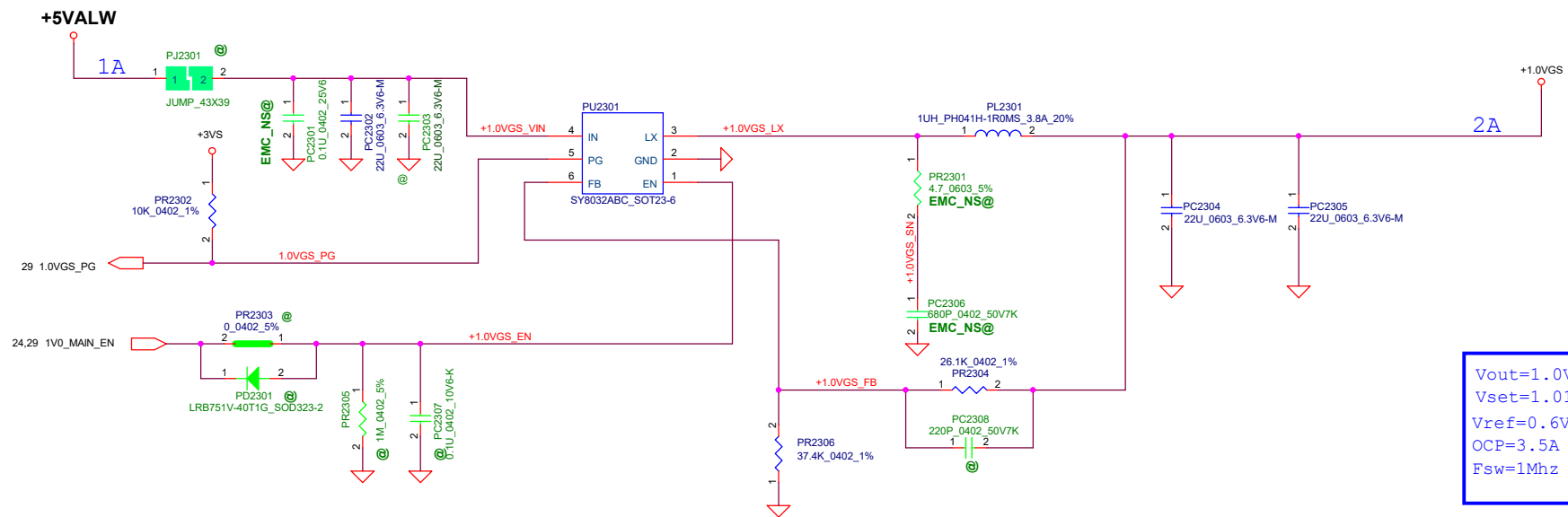
Y540:330u*2PCS+22u*19PCS
Y550:follow Y540 Vendor
PDG:470uF*4pcs+47uF*33pcs
Actual:330u*3PCS+22u*19PCS

Vboot=0V Loadline=1.1mG
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=10mV(0.5A-TDC)
Ripple=15mV(TDC-Iccmax)
TDC=125A Performance Line(5phase) Iccmax=165A
TDC=86A Base Line(4phase) Iccmax=140A
OVP=VIO+400mV
UVP=VID-300mV
Fsw=500Khz

Security Classification			LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Declassified Date	2018/08/02		PWR-VCCCPUCORE	
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Rev	1	Revised Number	Y550			51
Date	2018/08/02	Rev	1	Rev	1	51

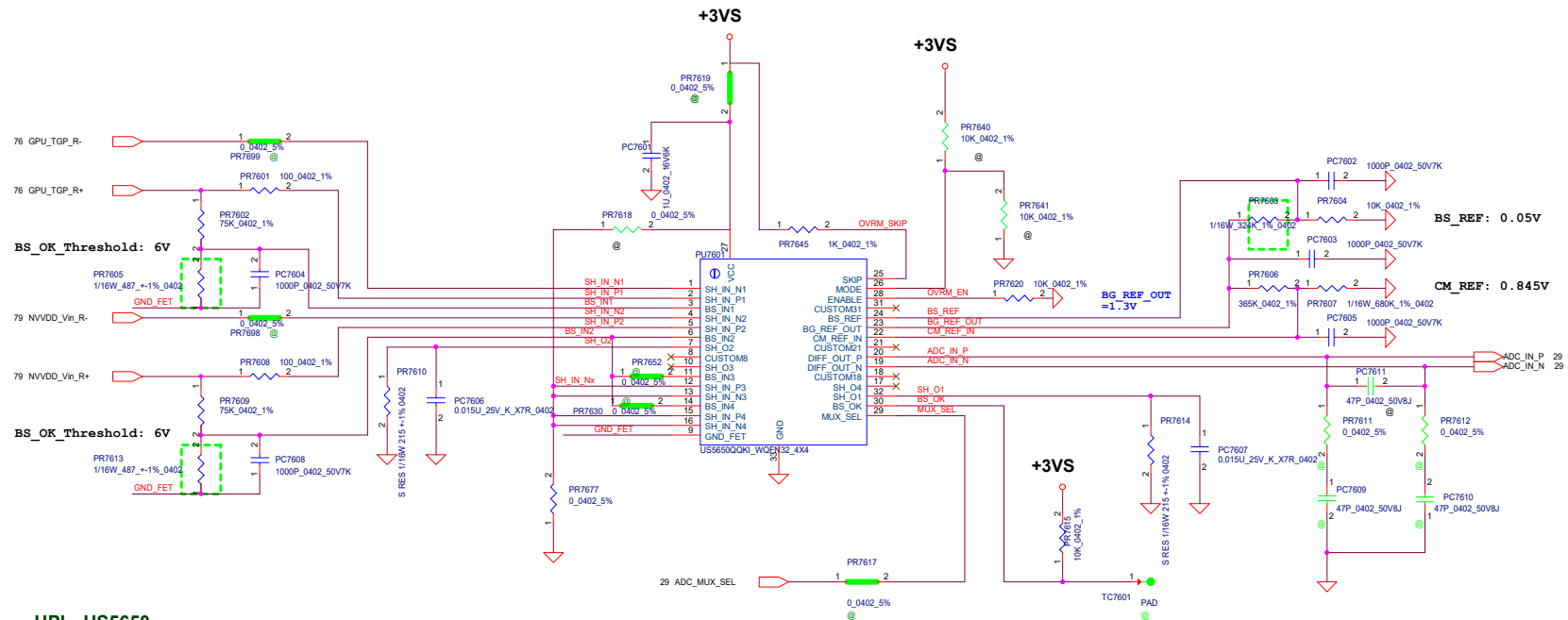
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM





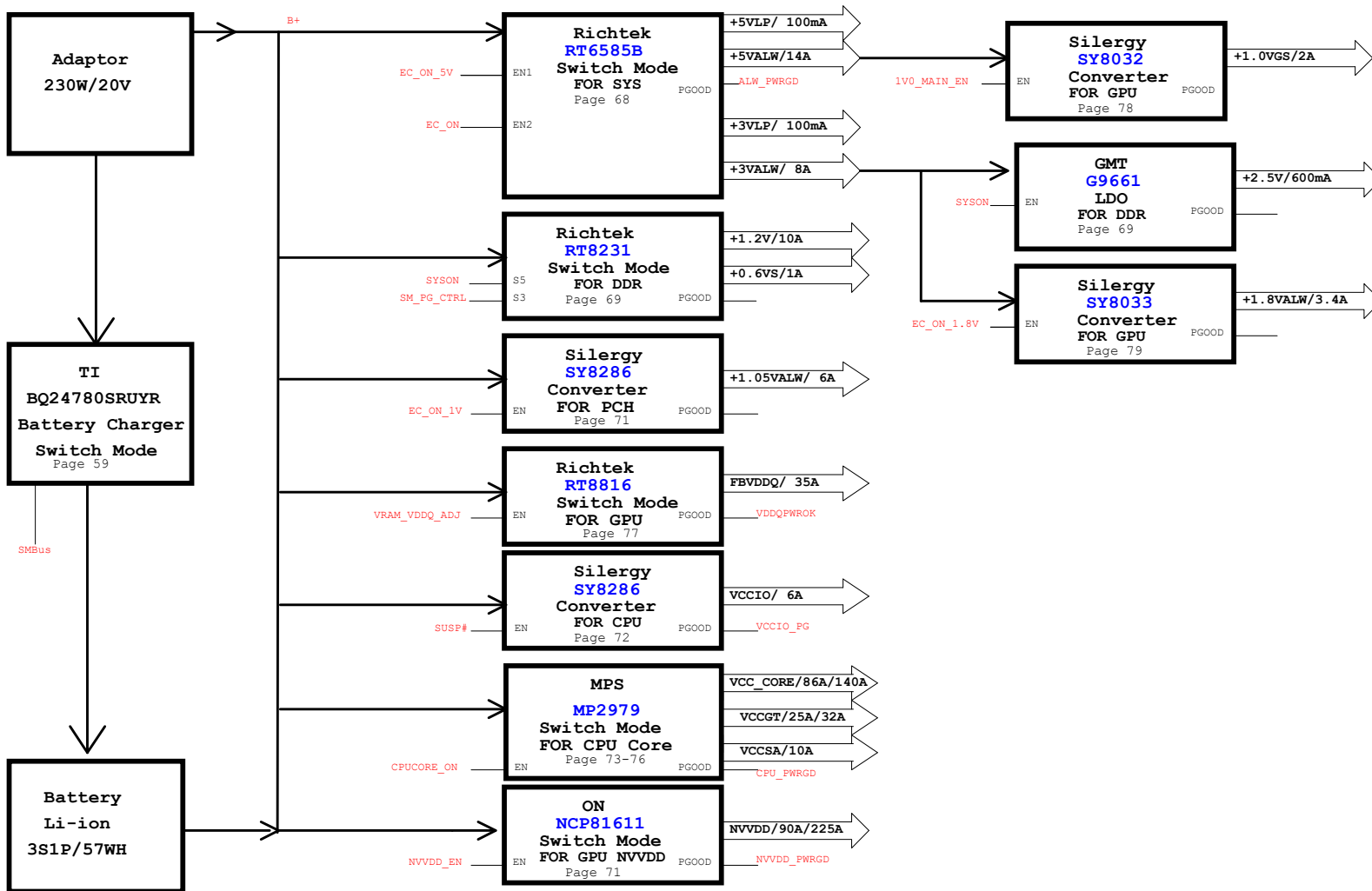
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UPI---US5650
 PR7605=487
 PR7613=487
 PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
 PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
 PR7603=324K
 PR7602=75K
 PR7609=75K
 PC7604=1nF
 PC7608=1nF

ON---NCP45491
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 PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
 PR7603=243K
 PR7602=75K
 PR7609=75K
 PC7604=1nF
 PC7608=1nF





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